EXHIBIT 24

UNITED STATES DISTRICT COURT

FOR THE EASTERN DISTRICT OF TEXAS

MARSHALL DIVISION

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NETLIST, INC.,	)	
Plaintiff.	)	
vs.	)	Case No.
MICRON TECHNOLOGY, INC.;	)	2:22-cv-203-JRG-RSP
MICRON SEMICONDUCTOR	)	
PRODUCTS, INC.; MICRON	)	
TECHNOLOGY TEXAS LLC,	)	
Defendants.	)	
_____	)	

VIDEOTAPED DEPOSITION OF HAROLD STONE, Ph.D.

REMOTE PROCEEDINGS

MONDAY, JUNE 26, 2023

STENOGRAPHICALLY REPORTED BY:

ANDREA M. IGNACIO, CSR, RPR, CRR, CCRR, CLR ~ CSR

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PAGES 1 - 208

A P P E A R A N C E S:

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ALSO PRESENT: Anthony Gulino, Videographer
Lance Hoeppner, Technician

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I N D E X

WITNESS: Harold Stone, Ph.D.

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REMOTE PROCEEDINGS

June 26, 2023 9:34 A.M.

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09:34

THE VIDEOGRAPHER: Good morning, everyone. 09:34
We are going on the record at 9:34 a.m. Pacific 09:34
Daylight Time on June 26, 2023. 09:34
Please note that this deposition is being 09:34
conducted virtually. Quality of recording depends on 09:34
the quality of camera and Internet connection of 09:34
participants. What is seen from the witness and heard 09:34
on screen is what will be recorded. 09:34
Audio and video recording will continue to 09:34
take place unless all parties agree to go off the 09:34
record. 09:34
This is Media Unit 1 of the video-recorded 09:34
deposition of Dr. Harold Stone, taken by counsel for 09:34
Plaintiff. 09:34
In the matter of Netlist, Inc. versus Micron 09:34
Technology, Inc., et al. Filed in the United States 09:35
District Court for the Eastern District of Texas, 09:35
Marshall Division. The case number is 2:22-CV-203 JRG 09:35
RSP. 09:35
This deposition is being conducted remotely 09:35
using virtual technology. 09:35
My name is Anthony Gulino, representing 09:35

Veritext Legal Solutions, and I am the videographer. 09:35
The court reporter is Andrea Ignacio from the 09:35
firm Veritext Legal Solutions. 09:35
I am not related to any party in this action, 09:35
nor am I financially interested in the outcome. 09:35
If there are any objections to proceeding, 09:35
please state them at the time of your appearance. 09:35
Counsel will now state their appearances and 09:35
affiliations for the record, beginning with the 09:35
noticing attorney. 09:35
MR. TEZYAN: This is Michael Tezyan from 09:35
Irell & Manella, representing Plaintiff Netlist. 09:35
MR. RUECKHEIM: Mike Rueckheim from Winston & 09:36
Strawn. And with me is Juan Yaquian, also from 09:36
Winston & Strawn, representing Micron and the witness. 09:36
THE WITNESS: I'm Harold Stone, the witness. 09:36
STENOGRAPHIC REPORTER: Are you done, 09:36
Mr. Videographer? 09:36
THE VIDEOGRAPHER: Yes, Andrea. 09:36
You can swear in the witness, please. 09:36
STENOGRAPHIC REPORTER: First, I need all 09:36
parties to agree that I'm in California, and the 09:36
witness is in Washington, and that it is okay for me 09:36
to swear in the witness, and that there will be no 09:36
objections? 09:36

MR. TEZYAN: That's fine. 09:36
THE WITNESS: No objection. 09:36
STENOGRAPHIC REPORTER: Mr. Rueckheim, I'm 09:36
sorry. I didn't hear you. 09:36
MR. RUECKHEIM: No objections. 09:36
STENOGRAPHIC REPORTER: Thank you.

HAROLD STONE, Ph.D.,
having been remotely sworn as a witness
by the Certified Shorthand Reporter,
testified as follows:

EXAMINATION

BY MR. TEZYAN:
Q Good morning. Can you please state your name 09:37
for the record. 09:37
A My name is Harold Stone. 09:37
Q Dr. Stone, have you been deposed before? 09:37
A Yes, I have. 09:37
Q How many times, approximately? 09:37
A It has to be approximate. I don't keep track 09:37
of the exact number, but several dozen. Let's just 09:37
say several dozen. 09:37
Q Fair enough. 09:37
Have any of those been virtual depositions? 09:37

A I believe this is my first. No, there was -- 09:37
I had one other. 09:37
Q Okay. I just bring that up to say that if 09:37
there are any, you know, technical difficulties as we 09:37
go on throughout the day, that's fine. It's 09:37
anticipated. 09:37
So you understand you're under oath? 09:37
A I understand. 09:37
Q And that the testimony you're going to give 09:37
today has the same effect as if you were in a court of 09:37
law? 09:38
A I understand that, yes. 09:38
Q Is there any reason you cannot give complete 09:38
and truthful testimony today? 09:38
A There is no reason. 09:38
Q If you answer a question, I will assume you 09:38
understood it; is that fair? 09:38
A Your audio is fading a little bit. Can you 09:38
repeat, please. 09:38
Q Sure. 09:38
My question was: If you answer my question, 09:38
I will assume you understood it; is that fair? 09:38
A That is fair, yes. 09:38
Q Okay. Are there any documents in the room 09:38
with you today? 09:38

A I -- you're asking, do I have any documents 09:38
in my room? 09:38
Q Yes. 09:38
A There are documents all over the place, none 09:38
of which I rely on and none of which I will use. 09:38
Q What's your setup like today? 09:38
A My setup today has a laptop that I'm facing. 09:38
When I turn like this, I'm looking at a large 09:38
replication of the screen. I'm sitting at a desk. 09:39
Off screen to my right, there is a printer 09:39
reader and a bookcase with books and other things and 09:39
loose papers, but none of which I will rely on. 09:39
Q Okay. So you don't have a printed copy of 09:39
your declaration in front of you? 09:39
A I do not. 09:39
Q Okay. Do you have any notes with you? 09:39
A I do not. 09:39
Q Okay. What did you do to prepare for today's 09:39
deposition? 09:39
A To prepare for this deposition, I read my 09:39
declaration. I read the patents at -- at -- in the 09:39
case. I read the materials cited in my depo- -- in my 09:39
declaration. That would include the materials 09:39
included by reference. And when I said "read," it's 09:40
more like scanned, because there's a lot of them. I 09:40

met with attorneys. 09:40
And that's -- that's about it. 09:40
Q What materials did you review in your 09:40
declaration in preparation for your deposition today? 09:40
A What materials did I review? 09:40
I reviewed my declaration. I reviewed the 09:40
reply brief from the -- from the litigants, reply from 09:40
Netlist. I reviewed the reply by Micron. I already 09:41
mentioned looking at the patents. 09:41
To my recollection, that's a fair 09:41
representation. I think I've covered them all, but I 09:41
might have missed something. 09:41
MR. TEZYAN: Now, if you'd go over to your 09:41
Exhibit Share and you go into the Marked Exhibits 09:41
folder, you'll see that I have premarked Exhibit 1. 09:41
Can you please pull up Exhibit 1. 09:41
(Document remotely marked Exhibit 1 09:41
for identification.) 09:41
THE WITNESS: Okay. 09:41
MR. TEZYAN: Q. And let me know when you 09:41
have it, sir. 09:41
A I have Exhibit 1. That's my declaration. 09:41
Q So Dr. Stone, what does it mean to convert a 09:42
voltage? 09:42
A Just a moment. I need to -- I'm going to 09:42

shrink this, if you don't mind. I'm going to get 09:42
the -- okay. Now I can look at you. 09:42
And you said, Dr. Stone, what do I mean by 09:42
convert -- convert -- I didn't get the word. 09:42
Converted or converter? 09:42
Q Sure. I'll repeat the question. 09:42
What does it mean to convert a voltage? 09:42
A What does it mean to convert a voltage? 09:42
It means to take an input voltage and to 09:42
change it into an output voltage. 09:42
Q Change it how? 09:42
A Depends on the converter. There are many 09:42
different ways. 09:42
Q So let's say we have a 5-volt input voltage, 09:42
and that's received by a component, which then outputs 09:42
a 3.3-volt output voltage. Is that conversion? 09:42
A That is. 09:42
Q What types of voltage conversion circuitry 09:43
would a person of ordinary skill in the art, at the 09:43
time of the '918 and '054 inventions, have been 09:43
familiar with? 09:43
A There are many different kinds of converters 09:43
that a person of ordinary skill in the art would know. 09:43
Q Can you give me some examples? 09:43
And feel free at any time to refer to your 09:43

dec- -- oh, I'm sorry. What is that? 09:43
A This is a voltage converter for USB. 09:43
Q Okay. 09:43
A It takes 110 volts in through these prongs 09:43
and produces a voltage out that will power -- let's 09:43
say it will recharge a phone. 09:43
Also, I'm on a laptop. The laptop runs on 09:43
DC. It's plugged into a voltage converter that's 09:43
plugged into the aux AC. 09:43
So those are two examples. 09:43
Q Okay. And what are those voltage 09:44
conversion -- sorry. Strike that. 09:44
Just generally, what kind of components are 09:44
voltage conversion circuits made up of? 09:44
A Generally, there are many different kinds of 09:44
components. It's -- it could be a long list. 09:44
But I would start with a transformer, for 09:44
example. In some instances, they use transformers. 09:44
It would have perhaps diodes, transistors, resistors, 09:44
inductors, capacitors, that type of thing. 09:44
Q Just a moment. I'm trying to introduce an 09:45
exhibit. 09:45
What about buck converters? What components 09:45
are those made up of? 09:45
A Well, there's a range of buck converters, and 09:45

they include the buck converter that would have an 09:46
inductor, capacitor, diode, perhaps, transistors. 09:46
Those are among the components that would be in a buck 09:46
converter. 09:46
Q And what do each of those components do? 09:46
For example, what does an inductor do? 09:46
A I left out switch. There would be a switch. 09:46
That would be the transistor. 09:46
But the -- the inductor reacts to change -- 09:46
voltage changes and to -- sorry -- to -- L di/dt is 09:46
the voltage across the inductor. So it responds to 09:46
the change of current and develops a voltage across 09:46
it. 09:46
Q And what does a capacitor do in the context 09:47
of a buck converter? 09:47
A Well, it stores charge and it smooths out 09:47
voltages. It controls the frequency of oscillation of 09:47
an LC circuit so that the -- the swings are at 09:47
frequencies that reflect the capacitance and the 09:47
inductance. So it has multiple functions. 09:47
Q And what does -- I believe you said a 09:47
transistor is another component in a buck converter; 09:47
correct? 09:47
A Yeah, I said that. It could be a diode or a 09:47
transistor. We need a switch of some sort. 09:47

Q Okay. And -- and what does the switch in the buck converter do?
A It switches the voltage on and off internally.
Q Got it.
What is the function of a resistor in a buck converter?
A It depends where it's located. But generally, I can talk about the function of a resistor. I don't know the structure that you're dealing with.
But the -- in typical situations, including those in a buck converter, a resistor would take -- carry current and have a voltage drop across it, and that voltage drop would affect the output voltage.
Q Are you familiar with boost converters, Dr. Stone?
A I am.
Q And what components comprise a boost converter?
A Actually, a boost converter would have roughly the same kinds of components that a buck converter would have. So everything I named for buck converter you might find in a boost converter, but the circuitry is different. So it's not the -- the

structure of a boost converter is not the same as the structure of a buck converter.
Q But both have defined structures; right, sir?
A Well, there are many ways you can build a boost converter and many ways you can build the buck converter. So I can't say that there is a single structure that covers either of them.
Q But both are understood to have common structural components; right?
A I believe that both -- a person of ordinary skill in the art would understand common components in a buck converter and common components in a boost converter.
Q And those are common structural components; right?
A Well, there's some aspects that are in common, but there's variations. So I don't know. I -- I can't answer your question specifically. I'm not sure how much variation you're allowing in the answer.
MR. TEZYAN: I've gone ahead and marked Exhibit 2, Dr. Stone.
Could you please refresh your Exhibit Share and let me know when you see Exhibit 2?
(Document remotely marked Exhibit 2

for identification.)
THE WITNESS: My monitor says it's coming up, but it's taking a while, so I'm not sure what's happening.
Ah, it's -- I have a message, "Generating file preview." May take a while.
MR. TEZYAN: Yeah, alternative to using the file preview, you can download the exhibit. It might be a little easier to do it that way.
THE WITNESS: I don't see a link for downloading, so --
THE VIDEOGRAPHER: Doctor, if you just --
THE WITNESS: Oh, I got it. Power Electronics. Page 1 of 37. It came up.
MR. TEZYAN: Great.
Q And Exhibit 2 is a book titled:
"Power Electronics: Converters, Applications, and Design. Second Edition."
Is that right?
A That's correct.
Q Can you please jump to page 165. And that's internal page number, so...
A I see page 1 of 37. So let's see how I can get to 165.
Q It's PDF page 20.

A 20. Got it.
Q Now, at the top, you see a circuit diagram, correct, right below where it says:
"7-3 Step-Down (Buck) Converter."
A "Step-down dc-dc converter."
7-4. I see that.
Q Oh, so I'm -- I'm talking about the -- yeah, so 7-4 (a), the figure that depicts the -- the circuit diagram.
Do you see that?
A I see that.
Q And this is a circuit diagram for a buck converter; right?
A That's what it claims. That's correct.
Q And the circuit diagram depicts an inductor, right, right above the L?
A I see that.
Q And there is a capacitor, the C; right?
A I see that.
Q And then there is a resistor to the right?
A I see that.
Q And these are all common structural elements for a buck converter; right?
A Oh, yes. I -- I believe that they're common in a buck converter, or at least that they're --

they're in this buck converter. 09:52
Q Can you please jump to PDF page 27. 09:53
A Okay. I'm there. 09:53
Q Do you see Figure 7-11 which says: 09:53
"Step-up dc-dc converter." 09:53
A I thought I was on page -- I'm sorry. No, I 09:53
see it. Okay. I'm in -- I'm on page 27, Figure 7-11. 09:53
I see that. 09:53
Q And another work -- another way to -- sorry. 09:53
Strike that. 09:53
A step-up dc-dc converter is otherwise known 09:53
as a boost converter; right? 09:53
A That's one name for it, yes. 09:53
Q And we see here in this diagram, Figure 7-11, 09:53
this is a circuit diagram for a boost converter; fair? 09:53
A I see that. 09:54
Q And we see that the boost converter comprises 09:54
a capacitor next to the C; right? 09:54
A I see that. 09:54
Q And then you have an inductor below the L on 09:54
the left; right? 09:54
A I see that. 09:54
Q And you have a resistor next to the R? 09:54
A I see that. 09:54
Q And these are all common structural elements 09:54

for a boost converter; right? 09:54
A I believe one of skill in the art would 09:54
understand these to be common in boost converters. 09:54
And certainly, they're in this boost converter. 09:54
Q Okay. So one of skill in the art would 09:54
understand that inductors, capacitors, and resistors 09:54
are common to both boost converters and buck 09:54
converters; fair? 09:54
A I think that's fair. 09:54
MR. TEZYAN: Okay. You can close out of 09:54
Exhibit 2. 09:54
THE WITNESS: Okay. 09:55
MR. TEZYAN: Q. So a buck boost converter is 09:55
another type of voltage conversion circuitry that a 09:55
person of ordinary skill in the art would have been 09:55
familiar with at the time of the '918 and 09:55
'054 patents; right? 09:55
A That's correct. 09:55
Q But what about an LDO? 09:55
A An LDO? That -- you're speaking of a low 09:55
dropout? 09:55
Q Yes. 09:55
A Okay. Low dropout. I believe that one of 09:55
skill in the art would know what an LDO converter is 09:55
at the time of the patents. 09:55

Q And if you'll just bear with me as I find 09:55
another exhibit. 09:55
And the function of an LDO, sir, is to 09:56
convert an input voltage into an output voltage; is 09:56
that correct? 09:56
A That -- that's largely correct. There may be 09:56
other stipulations about the nature of what the 09:56
conversion is. But that's basically what a general 09:56
statement of what an LDO converter does. 09:56
Q And to be more precise about it, an LDO will 09:56
convert an input voltage into a lower output voltage; 09:56
is that fair? 09:56
A I have not prepared to talk about LDO 09:56
converters. So to my knowledge, it might be correct. 09:56
But then again, there may be LDO converters that 09:56
increase voltage. But I'm not prepared to answer that 09:56
question based on what I prepared with regard to the 09:57
patents. 09:57
MR. YAQUIAN: Sorry. This is -- this is Juan 09:57
with Winston & Strawn. Sorry to cut off. Mike is 09:57
having depo -- Mike is having technical issues. He 09:57
needs to log on or re- -- log on or log off. So can 09:57
we just wait a moment? He needs to log off and log 09:57
back on. 09:57
MR. TEZYAN: That's fine. Let's go off the 09:57

record. 09:57
THE VIDEOGRAPHER: Okay. We're going to go 09:57
off the record. The time is 9:57 a.m. 09:57
And this is the end of Media No. 1. 09:57
(Recess taken.) 09:57
THE VIDEOGRAPHER: Okay. We are going back 10:20
on the record. The time is 10:20 a.m. 10:20
And this is the start of Media No. 2. 10:20
MR. TEZYAN: Welcome back, Dr. Stone. 10:20
Q Did you have any communications with your 10:20
counsel on the break? 10:20
A I did not. 10:20
MR. TEZYAN: If you go to your Exhibit Share 10:20
and refresh, you should see Exhibit No. 3. Please let 10:20
me know when you have it. 10:20
(Document remotely marked Exhibit 3 10:20
for identification.) 10:20
THE WITNESS: I must have lost my -- wait a 10:21
minute. I've got it. I -- I got the right web page. 10:21
I'm not clicking on Exhibit 3. I have Exhibit 3. 10:21
MR. TEZYAN: Okay. 10:21
Q And Exhibit 3 is a paper titled: 10:21
"Understanding Low Drop Out (LDO) 10:21
Regulators." 10:21
Right? 10:21

A That's correct. 10:21
Q And if you could please navigate to page 2. 10:21
A I am there. 10:21
Q At the bottom of page 2 is a circuit diagram 10:21
for an LDO; is that correct? 10:21
A I see that. That's correct. 10:21
Q And an LDO comprises a transistor switch; 10:21
right? 10:21
A The LDO comprises a transistor switch? Is 10:21
that what you said? 10:21
Q Yes, sir. 10:21
A I don't see a switch in this diagram. Are 10:22
you saying that this diagram has a switch? 10:22
Q Yes, that was the question. 10:22
A I don't see a switch. 10:22
Q Does an LDO generally comprise a transistor 10:22
switch? 10:22
A I'm not aware of an LDO with a transistor 10:22
switch. There may be some. As I indicated, I have 10:22
not prepared LDO material. 10:22
Q Dr. Stone, what is a circuit? 10:22
A That's a very general question. I believe 10:22
that the dictionary definitions I've seen presented to 10:23
me say that a circuit is a collection of components 10:23
that create a path, that type of thing; very generic, 10:23

of electrical components. 10:24
MR. TEZYAN: Q. So are you familiar with 10:24
registered DIMMs, Dr. Stone? 10:24
A And DIMM is D-I-M-M; is that correct? 10:25
Q Yes. It stands for dual in-line memory 10:25
module; right? 10:25
A Okay. I am familiar, yes. 10:25
Q You're familiar with registered DIMMs in 10:25
specific? 10:25
A Yes, I am familiar with registered DIMM, 10:25
D-I-M-M. 10:25
Q Right. 10:25
And a registered DIMM has a component on it 10:25
that's called a registered clock driver, right, 10:25
otherwise known as an RCD? 10:25
A I need a specific example, because I need to 10:25
know the -- the scope of your registered DIMM. The 10:25
clock driver may be on it or external to it. So I 10:25
can't answer your question as asked. 10:25
Q I'm sorry. Let me ask a foundational 10:25
question. 10:25
Do you know what an RCD is? 10:25
A Would you repeat the acronym. 10:26
Q Sure. 10:26
RCD stands for registering clock driver. 10:26

very general. I can't -- I -- I can't come up with a 10:23
firm definition -- (computer chiming) 10:23
STENOGRAPHIC REPORTER: I'm sorry. The bell. 10:23
"I can't come up with a firm definition" -- 10:23
THE WITNESS: Okay. I -- I can't come up 10:23
with a definition that will withstand scrutiny in all 10:23
cases. 10:23
MR. TEZYAN: Okay. 10:23
Q But what would a person of ordinary skill in 10:23
the art understand the term "circuit" to mean? 10:23
A I believe a person of ordinary skill will 10:23
understand a circuit to be a collection of 10:23
components -- electrical components. And beyond that, 10:24
there may be other aspects that would be in the 10:24
definition. But it would start with a collection of 10:24
electrical components connected together in some 10:24
fashion. 10:24
Q Okay. And those voltage conversion circuits 10:24
that we talked about, buck converters, boost 10:24
converters, LDO converters, would those be examples of 10:24
a collection of electrical components? 10:24
MR. RUECKHEIM: Object to the form. 10:24
THE WITNESS: I'm looking at this figure, and 10:24
I see electrical components, and I see a collection. 10:24
And so I believe that I would call this a collection 10:24

A Register and clock driver? 10:26
Q Registering clock driver. 10:26
A I know the acronym, but as you express it, 10:26
it's not firm in my mind what -- exactly what you 10:26
mean. A registered clock driver or -- I'm having 10:26
difficulty analyzing what your acronym is exactly. 10:26
Q Let's jump to your declaration, sir, if you 10:27
have it open. 10:27
A I don't have it open. I'm relying on you. 10:27
Oh, you want -- I'm sorry. It's my Exhibit 1; right? 10:27
Q Yes, sir. 10:27
A I have -- I have Exhibit 1 open. 10:27
Q Let's jump to PDF page 23. 10:27
A That's the page that says PDF page 23? 10:27
Q Uh-huh. 10:27
A Okay. It -- 10:27
Q So underneath "Corresponding Structure," you 10:27
use a term called "memory module controller." 10:27
Do you see that? 10:27
A I see that. 10:27
Q What does that mean? 10:27
Is that referring to, for example, 10:27
controller 1062 in the '918 patent? 10:28
A The memory module controller, I believe, is 10:28
1062, but I'd have to take a moment to just confirm. 10:28

If you don't mind bringing up the '918 patent so I can confirm the 1062 is the memory module controller, that would be helpful.

MR. TEZYAN: Sure. Okay.

Please refresh your Exhibit Share, and let me know when you see Exhibit 4.

THE WITNESS: Okay. I have refreshed.

(Document remotely marked Exhibit 4 for identification.)

THE WITNESS: I have the exhibit.

MR. TEZYAN: Q. What is Exhibit 4?

A Exhibit 4 is the '918 patent. It's taking a while to come up, so I don't see it yet. I've got the message saying the file created may take a while, but it's coming.

It's here. I have it.

Q Okay. And can you please confirm, now that you have it, that Exhibit 4 is the '918 patent?

A I confirm that Exhibit 4 is the '918 patent.

Q And -- and take your time to review it, sir, if you need to to refresh your memory.

But the question was, just to remind you, is the memory module controller that you referred to in your declaration controller 1062?

A Just a moment.

It is 1062. That's correct.

Q Okay. Thank you.

I'm going to go ahead and introduce Exhibit 5.

(Document remotely marked Exhibit 5 for identification.)

MR. TEZYAN: Q. Please refresh your Exhibit Share, and let me know when it comes up.

A I have started the load. I have an indication that the load is occurring. Again, I have the message that says that the file preview may take a while.

Q That's fine.

When it comes up, can you please go to PDF page 10.

A Okay.

Q And before that, I should ask, if you go back to page 1, can you please confirm that this is the JEDEC 21-C "DDR SDRAM Registered DIMM Design Specification"?

A I will confirm that when I see it.

Q Fair enough.

A It just came up.

Q Okay.

A Okay. I see that this is the "DDR SDRAM

Registered Design Specification" dated January 2002.

I'm now going to go to page 10.

I have page 10.

Q And on page 10, depicted here is a block diagram for a particular Raw Card configuration; is that right?

A That's correct.

Q Okay. And if you go to the bottom left corner of page 10, you see this diagram that includes a register with signals coming in on the left and another set of signals going in on the right?

A I see that.

Q Okay. And the register that's depicted here is a circuit; correct?

A That's correct.

Q Now, the '918 patent discloses in the specification various examples of the controller; is that correct?

A "The controller" being the memory controller 1062. And it -- it is correct that there are examples of the memory controller in the '918 patent.

Q And an FPGA is one of those examples; right?

A I -- would you say that again, please. I didn't get the acronym.

Q Sure.

An FPGA is one --

A An FPGA. Yes, I believe that's the case. FPGA is an example. It's -- the way it is displayed, it doesn't -- it's not indicative that it's the whole memory controller. But it -- it -- there is a memory controller that comprises an FPGA.

Q Okay. And what is an FPGA?

A An FPGA is a field programmable gate array.

Q What is it comprised of?

A Well, there are many different FPGAs. Normally, it has gates within it. It has a programming structure that allows external volts, external voltages to cause changes in the FPGA so that it can become different circuits, depending on the programming.

Q Okay. So an FPGA has to be comprised of some type -- some type of circuitry; is that right?

A That's correct.

Q And what kind of circuitry is that?

A Well, it varies across FPGAs. The circuitry at the lowest level would involve conductors and some sort of devices that allow it to be programmed. They could be fuses, for example, or they could be devices that assume a state and retain that state when -- when

volts -- when power is removed. 10:38
And beyond that, the components of an FPGA 10:38
are whatever people choose to put into it. 10:38
Q And what is an ASIC, sir? 10:38
A ASIC is A-S-I-C, application-specific 10:38
integrated circuit. 10:38
Q And what is an ASIC comprised of? 10:38
A Well, it's comprised of whatever the designer 10:38
chooses to put into it. Be- -- because it is 10:38
application-specific, different applications will use 10:38
different components in ASICs built for those 10:39
applications. So I can't tell you exactly what is in 10:39
an ASIC. 10:39
Q Were you finished with your answer, sir? 10:39
A I -- I -- would you repeat your question. 10:39
Q Oh, I'm sorry. I felt as if I almost cut you 10:39
off. I just wanted to know if you were finished with 10:39
your answer. 10:39
A I -- I'm done with my answer. 10:39
Q Okay. But an ASIC is still an integrated 10:39
circuit; right? 10:39
A It is an integrated circuit. That is 10:39
correct. 10:39
Q There is -- there is -- there are certain 10:39
circuitry that has to be common to all ASICs; right? 10:39

At the very least, conductors and -- and that 10:39
sort of low-level circuitry; right? 10:39
A You used the word "all," some things common 10:39
to all ASICs. I can't testify that every ASIC has 10:39
some specific thing in it because of the wide -- wide 10:39
variety. 10:39
Q Are there some ASICs that are not integrated 10:39
circuits? 10:40
A I believe that all ASICs are integrated 10:40
circuits, yes. 10:40
Q And integrated circuits have common low-level 10:40
components to them; is that fair? 10:40
A I don't think that's fair. 10:40
Q Can you explain? 10:40
A May I give an example? 10:40
Q Please. 10:40
A A quantum computer circuit may not have any 10:40
components in common with an ASIC that you have, and 10:40
yet the quantum computer ASIC is an ASIC. 10:40
Q Fair enough. 10:41
What about ASICs designed specifically for 10:41
the use in memory modules? Would those integrated 10:41
circuits have components in common? 10:41
MR. RUECKHEIM: Object to the form. 10:41
THE WITNESS: If you present a memory 10:41

device A and a memory device B and ask the question, 10:41
do these two devices have elements in common, I would 10:41
be able to look and investigate. 10:41
I -- your -- your question is so broad, I'm 10:41
not sure that I can answer it. 10:41
(Document remotely marked Exhibit 6 10:42
for identification.) 10:42
MR. TEZYAN: I'm introducing Exhibit 6. 10:42
Q Dr. Stone, could you please refresh your 10:42
Exhibit Share, and let me know when you see Exhibit 6. 10:42
A I am -- I see the list that says Exhibit 6. 10:42
I'm clicking on the link. My screen shows that the 10:42
PDF file is loading. 10:42
I have it. 10:43
Q Okay. So Exhibit 6 is titled: 10:43
"LatticeXP2 Family Data Sheet Introduction." 10:43
Is that right? 10:43
A That's correct. 10:43
Q And it's dated May 2007; right? 10:43
A May 2007. That's correct. 10:43
Q If you'd go to page 2. And you can read that 10:43
first sentence below "Introduction" to yourself. 10:44
A (Reading document.) 10:44
I see that. 10:44
Q This is an example of an FPGA that's designed 10:44

by Lattice; right? 10:44
A I have not seen this document before. But if 10:44
that's what you say it is, I -- I -- I say that it's 10:44
consistent with what you represent. 10:44
Q Well, that first sentence says: 10:44
"LatticeXP2 devices combine a Look-up 10:44
Table" -- "based FPGA fabric with non-volatile Flash 10:44
cells in an architecture referred to as flexiFLASH." 10:44
Right? 10:44
A I see that, yes. 10:44
Q And the document is titled: 10:44
"LatticeXP2 Family Data Sheet Introduction." 10:44
Right? 10:45
A Yes. 10:45
Q So fair to say that this is a data sheet for 10:45
a Lattice FPGA? 10:45
A That's what you're representing. I -- I 10:45
don't dispute that. 10:45
Q Let's go to page 4 of this document. 10:45
A I'm on page 4. 10:45
Q And you see Figure 2-1 is a block diagram of 10:45
the LatticeXP2 device; right? 10:45
A XP2-17. Yes. 10:45
Q Correct. 10:45
And you see that the device is comprised of 10:46

several components; right? 10:46
A I see that, yes. 10:46
Q And that includes flash; right? 10:46
A I'm looking. It says, yes, flash. 10:46
Q Flash is a type of nonvolatile memory; right? 10:46
A That's correct. 10:46
MR. TEZYAN: Okay. We can close out 10:46
Exhibit 6. 10:46
Q Now, what would a person of ordinary skill in 10:46
the art understand the term "controller" to mean? 10:46
A The term "controller" is very general. Let 10:46
me give an example from the patents. Let's see. We 10:47
have the '918 patent. May I bring it up? 10:47
Q Yes. It's Exhibit No. 4. 10:47
A Exhibit -- yeah, I -- I'm going to back away 10:47
from that. 10:47
It -- a controller is basically something 10:47
that controls. But beyond that, it's not at all clear 10:47
what the specifics of a controller are. 10:47
So I -- I don't know exactly what one of 10:47
skill in the art would understand a controller to be, 10:47
beyond a device or something that does the control 10:47
function. 10:48
Q Okay. But a controller is an electronic 10:48
device; fair? 10:48

MR. RUECKHEIM: Object to the form. 10:48
THE WITNESS: Among the universe of 10:48
controllers, some are electronic devices, but not all. 10:48
MR. TEZYAN: Okay. 10:48
Q Well, in the context of memory modules, a 10:48
controller specifically for use in a memory module 10:48
would be an electronic device; fair? 10:48
A A memory controller -- a controller for a 10:48
memory device would be electronic. I believe that's 10:48
fair, yes. 10:48
Q Okay. And electronic devices generally have 10:48
certain low-level components in common, right, such as 10:48
the ones we talked about earlier, like conductors? 10:48
A Certain, yes. But even memory devices -- 10:48
device memory A and device memory B may have nothing 10:48
in common; very little in common, if anything. 10:48
Q Okay. But controllers for memory modules 10:49
specifically, they would have at least certain aspects 10:49
in common, right, like -- I'm sorry. Strike that. 10:49
So do -- do we agree that controllers for 10:49
memory devices comprise conductors, at least? 10:49
A Conductors being a metal of some sort that 10:49
conduct electricity. 10:49
Is that what you mean? 10:49
Q Yes. 10:49

A They would have conductors, yes. 10:49
Q Okay. Would controllers for memory devices 10:49
have other components in common? 10:49
A I don't see why they should. 10:49
Q Okay. But a controller performs the function 10:50
of, I think you said, something that controls -- so 10:50
strike that. Sorry. 10:50
And I think we can agree that a controller 10:50
performs the function of controlling some other 10:50
component; is that fair? 10:50
A I don't even know that it controls some other 10:50
component. It controls. That's fair. 10:50
Q Okay. It controls something; right? 10:50
A Something. That's right. 10:50
Q Okay. And would that something have to be 10:50
something other than itself? 10:50
A I'm not sure. 10:51
Q Let me rephrase the question. 10:51
Would a person of ordinary skill in the art 10:51
typically understand a controller to be a device that 10:51
controls something other than itself? 10:51
A I think that's a fair understanding of a 10:51
person of skill in the art. 10:51
But if you ask me if there are instances 10:51
where it can control itself, that would be an 10:51

interesting question. It might still be a controller 10:51
controlling only itself. 10:51
Q Fair enough. 10:51
But typically, a person of ordinary skill in 10:51
the art would understand that a controller is a device 10:51
that controls some other component; right? 10:51
A I think we're talking about typically or in 10:51
general, but not necessarily every case. 10:51
Q Okay. And in order to control some other 10:51
component, the controller has to be connected to that 10:51
component; is that fair? 10:51
A I don't fully know your context. I can give 10:52
examples where it's not connected. 10:52
Q Okay. And in what way can a controller not 10:52
be connected to the -- 10:52
A I have wireless chargers, for example. 10:52
They -- you put a device inside the wireless charger 10:52
and it charges up. The wireless charger is 10:52
controlling the device that's being charged. There is 10:52
no connection. 10:52
Q Okay. Outside the context of wireless 10:52
communications or charging, a controller necessarily 10:52
has to be connected to the item that it's controlling? 10:52
A You keep -- you keep saying things like 10:52
"necessarily" or "all" or whatever, and it -- it 10:52

bothers me. 10:52
I would say that a controller is usually 10:52
connected to the thing that's controlled, but I would 10:52
be hard pressed to say in every case. 10:53
Q Okay. Well, in the context of controllers 10:53
that are designed for memory modules, the controller 10:53
which is controlling components on the memory module 10:53
would have to be connected to those components; is 10:53
that fair? 10:53
A I just gave an example of wireless chargers 10:53
for, let's say, a cell phone. A cell phone has 10:53
memory. A controller is not connected to that cell 10:53
phone as you say "connected." It's wirelessly 10:53
influencing and controlling it. 10:53
So you keep -- with this discussion, we're -- 10:53
every instance is covered by your -- your request. I 10:54
can't -- I can't acknowledge that every instance does 10:54
what you say it does. 10:54
MR. TEZYAN: Okay. Well, I'll object that 10:54
that's nonresponsive, and I'll move to strike. 10:54
Q So the question was: In the context of 10:54
controllers that are designed for memory modules, the 10:54
controller which is controlling components on the 10:54
memory module would have to be connected to those 10:54
components; is that fair? 10:54

A You said now -- 10:54
MR. RUECKHEIM: Objection to the form. 10:54
You can answer. 10:54
THE WITNESS: Your question says now the 10:54
controller is on the memory module; is that correct? 10:54
MR. TEZYAN: Yes. 10:54
THE WITNESS: In that instance, it is fair to 10:54
say that that memory controller on the memory module 10:54
is connected to the memory. 10:54
MR. TEZYAN: I'm sorry. I think something 10:54
got lost in translation there. 10:54
Q So the question was -- and I'll just repeat 10:55
it again: In the context of controllers that are 10:55
designed for memory modules, the controller which is 10:55
controlling components on the memory module would have 10:55
to be connected to those components; fair? 10:55
A I believe that's -- that's fair, yes. I 10:55
would say that's fair. 10:55
MR. TEZYAN: Okay. Let's take a break. 10:55
THE VIDEOGRAPHER: We are going to go off the 10:55
record. The time is 10:55 a.m. 10:55
And this is the end of Media Unit No. 2. 10:55
(Recess taken.) 10:55
THE VIDEOGRAPHER: We are going back on the 11:15
record. The time is 11:15 a.m. 11:15

And this is the start of Media Unit No. 3. 11:15
MR. TEZYAN: Welcome back, Dr. Stone. 11:15
Q Did you have any communications with counsel 11:15
during the break? 11:15
A I did not. 11:15
Q You've been retained by Micron as an expert 11:15
in this case; right? 11:15
A That's correct. 11:15
Q And you've been retained to opine on 11:15
technology that's present in certain patents invented 11:15
by Netlist? 11:15
A Yes, it's correct. I -- I should look at my 11:15
retention letter if it -- if it matters exactly what 11:15
the details, but that's the general gist of my 11:15
retention. 11:15
Q This isn't the first time you've been adverse 11:15
to Netlist; is that fair? 11:15
A To Netlist, yes. I'll say yes to Netlist. 11:16
Q That's yes, you've been adverse to Netlist in 11:16
the past? 11:16
A Not exactly. I think the patents in question 11:16
were owned by another party. The -- the patents may 11:16
have inventors who were Netlist inventors. The 11:16
parties involved did not involve Netlist. 11:16
Q Okay. Let's go down to PDF page 30 of your 11:16

declaration. That's Exhibit 1. 11:16
A Okay. 11:16
Q And at the very bottom of PDF page 30, 11:16
there's a number of IPRs listed there. And then it 11:17
says: 11:17
"SK hynix v. Netlist, testifying for 11:17
SK hynix." 11:17
Do you see that? 11:17
A I don't see it yet. It's reloading. It will 11:17
come up shortly. It's still loading. 11:17
Q And since we'll be coming back to your 11:18
declaration throughout the day, it might just be more 11:18
efficient to download it just so you have a local copy 11:18
that you can come back to. 11:18
A Okay. And what do -- you want me to download 11:18
this one? I don't see a click -- a way to click on it 11:18
to download it. 11:18
Q It should be in the top right corner. 11:18
THE VIDEOGRAPHER: Counsel, if he's using the 11:18
guest version, he can't download. 11:18
MR. TEZYAN: Okay. 11:18
THE WITNESS: Oh, the upper-right corner? 11:18
There is a -- let's see what I have. 11:18
Ah, I got it. Okay. So I clicked on it, but 11:18
it just brought it up. Okay. I -- I have not 11:18

downloaded, but I see it now. 11:18
MR. TEZYAN: Okay. 11:18
Q And you're at the bottom of PDF page 30; is that right? 11:18
A I'll have to get there. 11:18
I'm on page 30. My page 30 is my -- is my CV. 11:19
Q Right. 11:19
And at the bottom, it -- it says: "Consultantships." 11:19
And it lists a number of cases that you've worked on in the past; is that right? 11:19
A That's correct. That's correct. 11:19
Q And it lists that you were an expert consultant working on a number of IPRs for the Sidley Austin firm; is that right? 11:19
A That's correct. 11:19
Q And sort of near the bottom, you see it says: "SK hynix v. Netlist, testifying for SK hynix." 11:19
And before that, there are six IPR numbers listed? 11:19
A Yes. All right. 11:19
There was an interesting thing that happened in that case. The ownership -- as I recall, the 11:19

patents got changed. Initially, it was a tribe, or at some point it was a tribe. So I -- I -- this is what I was thinking about. The patents were -- were Netlist type of patents. 11:19 11:20 11:20
But you see -- oh, down on beginning of page 3, it says: 11:20
"Microsoft v. St. Regis Tribe." 11:20
That was also involved somewhere along the line. 11:20
So I was testifying for SK hynix at the IPR as a petitioner, and the patent owner was Netlist. That's correct. 11:20 11:20 11:20
Q Okay. So just to re-ask my question for clarity of the record, you've been adverse to Netlist on several occasions in the past; correct? 11:20 11:20
A Let's just say that I've been adverse to Netlist on occasions according to my consultantships. I can't -- I don't want to use the word "several" or "few" or "any." Just -- the facts are in the curriculum vitae. 11:20 11:20 11:20 11:21
Q Okay. And one of the proceedings listed in your CV is "IPR 2018-00363"; correct? 11:21 11:21
A Yes. 11:21
MR. TEZYAN: Okay. Go ahead and refresh your Exhibit Share for me. I've marked Exhibit 7. 11:21 11:21

(Document remotely marked Exhibit 7 for identification.) 11:21 11:21
THE WITNESS: Okay. Oh. 11:21
MR. TEZYAN: Q. Let me know when you have it. 11:21 11:22
A It's coming. It's one of these things that take a while. It just produced that error message or the wording message that the file preview may take a while. 11:22 11:22 11:22
Q While that's loading, sir, I believe you testified earlier that in preparation for this deposition, you had reviewed the parties' briefs submitted in this case; is that correct? 11:23 11:23 11:23 11:23
A That's correct. That's the reply brief that says you can -- just a moment. It says the file preview generation is still in progress. You can stay on this page and keep retrying, or exit preview and return at a later time. It gives me a button called reload. 11:23 11:23 11:24 11:24 11:24 11:24
Shall -- what shall I do? 11:24
MR. TEZYAN: Can the tech please advise? 11:24
THE WITNESS: I'm sorry. Say again, please. 11:24
THE VIDEOGRAPHER: Yeah, I mean, this is kind of what I was talking about. His computer is just slow. So, I mean, if you want to screen share certain 11:24 11:24 11:24

documents that are larger, it might just be faster to do that. 11:24 11:24
THE WITNESS: To -- to download? 11:24
MR. TEZYAN: All right. 11:24
I'll go ahead and screen share this one. 11:24
Well, you know what? Let's go off the record for a second. 11:24 11:24
THE WITNESS: Okay. 11:24
MR. RUECKHEIM: That's fine. 11:24
THE VIDEOGRAPHER: We are going off the record. The time is 11:24 a.m. 11:24 11:24
And this is the end of Media Unit No. 3. 11:24
(Recess taken.) 11:25
THE VIDEOGRAPHER: We are going back on the record. The time is 11:29 a.m. 11:29 11:29
And this is the start of Media Unit No. 4. 11:29
MR. TEZYAN: Q. So do you recognize Exhibit 7, Dr. Stone? 11:29 11:29
A I do. 11:29
Q And Exhibit 7 is a declaration you submitted in IPR2018-00363; is that correct? 11:29 11:29
A That is correct. 11:30
Q And I think before the break, I had asked you if you had reviewed the parties' briefs in this case in preparation for your deposition. 11:30 11:30 11:30

But just to be more specific, have you 11:30
reviewed Micron's responsive brief as well? 11:30
A I have reviewed Micron's responsive brief, 11:30
yes. 11:30
Q Okay. So you understand that one of the 11:30
issues in this case is whether the '339 patent is 11:30
directed to what's called a "fork in the road"; right? 11:30
A That's correct. 11:30
MR. RUECKHEIM: Objection to form. 11:30
MR. TEZYAN: Q. And that's an issue you've 11:30
encountered before; right? 11:30
A That's correct. 11:30
Q Okay. And if we can jump to paragraph 63 of 11:30
this declaration, sir. Let me know when you're there. 11:30
A I have -- I've got the wrong one. 11:31
Q It's on PDF page -- 11:31
A Exhibit 7. I've got it. 11:31
Q Okay. 11:31
A Okay. Now, we're going to paragraph what? 11:31
Q Paragraph 63. It's on PDF page 30. 11:31
A I've got -- let's see. I have paragraph 63. 11:31
Q Okay. And here, it says the word -- the 11:31
phrase "fork in the road" is used: 11:31
"As a non-technical shorthand to refer to 11:31
this switching action by data transmission circuit 416 11:31

between data path A and data path B." 11:31
Do you see that? 11:31
And it's referring to data path A and data 11:31
path B in Figure 5 that's on the next page. 11:31
A Okay. I understand that in prior litigation 11:31
between the parties involving the '185 patent, which 11:31
is the parent to the '907 patent, they used the phrase 11:32
"fork in the road." Okay. I see that. 11:32
Q And do you see Figure 5 below on the next 11:32
page? 11:32
A Yes, I see Figure 5. 11:32
Q And do you see the blue arrow going through 11:32
what is data path A that connects to terminal Y1? 11:32
A I do. 11:32
Q And then the data path extending from 11:32
terminal Y1 to "Memory Ranks A, C"? 11:32
MR. RUECKHEIM: Object to the form; beyond 11:32
the scope. 11:32
THE WITNESS: No. There are two parts of a 11:32
figure here. You have to help me. 11:32
Repeat your question again, please. 11:32
MR. TEZYAN: Q. Oh, I'm just asking if you 11:32
see that the data path extends from terminal Y1 to 11:32
Memory Ranks A and C? 11:33
A And you're referring to the upper figure or 11:33

to the lower figure? 11:33
Q Oh, to the upper figure, sir. 11:33
A I see that. 11:33
Q Okay. And then you have sort of in 11:33
light-shaded blue a data path that goes below A and 11:33
that's labeled "B"; right? 11:33
A I see the path. What did you say the label 11:33
was? 11:33
Q Oh, it's labeled "B." 11:33
A I see the B. It's okay. 11:33
Q Okay. 11:33
A I see. 11:33
Q So we have data path A and data path B; 11:33
right? 11:33
Just trying to set the table. We -- we both 11:33
have a common understanding of this figure. We have 11:33
data path A and data path B; right? 11:33
MR. RUECKHEIM: Object to the form; beyond 11:33
the scope. 11:33
THE WITNESS: I -- I have to see the context. 11:33
I'm -- I'm struggling, because A and B are connected. 11:34
Usually when you have a separate data path, there is 11:34
an intermediate component. 11:34
MR. TEZYAN: Okay. 11:34
Q But you see that there is this triangle 11:34

labeled 504; right? 11:34
A I do. 11:34
Q And triangle 504 is a tristate buffer; right? 11:34
MR. RUECKHEIM: Object to the form; beyond 11:34
the scope. 11:34
THE WITNESS: Yeah, 504 is a tristate buffer. 11:34
MR. TEZYAN: Okay. 11:34
Q And 506 is a tristate buffer as well; right? 11:34
A I believe that's the case. 11:34
Q Okay. And the tristate buffer in data 11:34
path B, that's tristate buffer 506, has an X through 11:34
it; right? 11:34
A This is not completely clear to me, because 11:34
there are three things that you were referring to by 11:35
saying "X." There is an input to X, there is X, and 11:35
the output. And I'm -- your question is not clear to 11:35
me as to what is what. 11:35
Q Okay. Well, why don't we jump to 11:35
paragraph 64, and that's on PDF page 32. 11:35
A Okay. 11:35
Q And it says: 11:35
"When the control logic circuitry 502 11:35
receives" -- "an 'enable A' signal, a first tristate 11:35
buffer 504 in path A" -- "is enabled and actively 11:35
drives the data value on its output, while a second 11:35

tristate buffer 506 in path B is disabled with its output in a high impedance condition." 11:35
Did I read that correctly? 11:36
A I believe you have. I'm -- I'm reading it again just to make sure I got all the words. 11:36
Q Yeah, take your time. 11:36
A I understand. Okay. You -- I believe you read it correctly, but let's go ahead. 11:36
Q Okay. And returning to that annotated version of Figure 5 that appears on PDF page 31 of your declaration. 11:36
A Okay. 11:36
Q The -- sorry. Withdraw. 11:36
So data paths A and B are two prongs of the fork in the road; right? 11:36
MR. RUECKHEIM: Object to the form, and beyond the scope. 11:37
And Counsel, Dr. Stone has not opined on the '339 patent that involves the fork in the road. Can you confirm your questions have nothing to do with his claim construction declaration for the record? 11:37
MR. TEZYAN: Counsel, I'm going to read to you Local Rule CV 30, and that says: 11:37
"Objections to questions during the oral deposition are limited to objection; leading and 11:37

objection; form." 11:37
Going forward, I'd appreciate it if you complied with that rule. 11:37
MR. RUECKHEIM: Understood. 11:37
Dr. Stone, you can answer this question. Then we'll take a break, and we can talk offline. 11:37
THE WITNESS: Did you say I can answer the question, and then -- 11:37
MR. RUECKHEIM: If you can. 11:37
THE WITNESS: Okay. Would you ask the question again? 11:37
MR. TEZYAN: Sure. 11:37
Q The question was: Data path A and B are two prongs of the fork in the road; right? 11:37
And if you need to remind yourself, you can go ahead and review paragraph 63 of your declaration. 11:38
A Did your question end at that point? 11:38
I'm sorry. You're -- you're asking me that A and B are two -- two prongs of the fork; is that correct? 11:38
Q Yes, sir. 11:38
A Okay. My reading of my declaration is informed by the end of paragraph 64. And I'm looking at the fifth line, a sentence that begins "similarly": 11:38
"Similarly, if an 'enable B' signal is 11:39

received, the first tristate 504 opens path A and the second tristate 506 closes path B" -- "thus directing the data to a second terminal Y2." 11:39
Okay. Let's just stop there, and I'll go back to the figure. And we're going to the figure. 11:39
So according to that reading, the second path on that fork comprises the part that is the input to the tristate driver that has an X on it, and continues through Y2, and then onto the Memory Ranks 452. That's the path. And the 506 interrupts the path. 11:39
Now, your question -- if you can repeat your question, I can try again to answer it. 11:40
Q Sure. 11:40
The question was just: Are A and B the two prongs in the fork in the road that the parties previously have used as a shorthand for that switching action between paths A and B? 11:40
MR. RUECKHEIM: Object to the form. 11:40
THE WITNESS: I have difficulty, because B is part of a path. And when you say "prong," I don't -- I am uncertain if you mean the whole path, which is what the patent talks about, or just the little bit that goes to the tristate driver with the X. 11:40
If you talk about prongs, I -- reading the patent, I would believe you're talking about paths, 11:41

but I don't know. I can't -- can't -- I can't answer your question. 11:41
MR. TEZYAN: Sure. Sure. 11:41
Q If you could answer the question assuming I mean paths. 11:41
So are -- are A and B two different paths in that fork? 11:41
A A -- 11:41
MR. RUECKHEIM: Same objection. 11:41
THE WITNESS: -- A is the path that goes to the memory and includes the part that goes to the memory. B is the path that goes to Memory Ranks B and D and includes that part. Those two are paths. 11:41
MR. TEZYAN: Okay. 11:41
MR. RUECKHEIM: We can break. 11:41
MR. TEZYAN: No. 11:41
MR. RUECKHEIM: We can go off the record right now. 11:41
THE VIDEOGRAPHER: We need both parties to -- 11:41
MR. TEZYAN: I'm going to jump to his actual declaration now in this action. So if we could just go to that real quick. 11:41
MR. RUECKHEIM: Understood. Go ahead. 11:41
MR. TEZYAN: Okay. 11:42
Q Dr. Stone, can you go back to Exhibit 1, 11:42

please? 11:42
A Okay. I was -- go back to what? 11:42
Q Exhibit No. 1, sir, your -- 11:42
A Exhibit No. 1. 11:42
Q -- declaration for this -- 11:42
A Okay. 11:42
Q -- claim construction brief. 11:42
A Got it. Okay. 11:42
Q And can you go to paragraph 25, please. 11:42
A Just a moment. There's my declaration. 11:42
25 paragraph? 11:42
Q Yeah. It's on PDF page 10. 11:42
A I have it. 11:42
Q Okay. So you say that a person of ordinary 11:42
skill in the art would have been familiar with 11:42
standardized DRAM, SDRAM memory devices, memory 11:43
modules, and how they interacted with the memory 11:43
controller and other parts of a computer system. 11:43
Do I have that right? 11:43
A You have that correct. 11:43
Q Okay. So what is load? 11:43
A Load has variable meanings, multiple 11:43
meanings, and you have to determine what load means 11:43
from the context in which you use it. 11:43
Q Okay. Fair enough. 11:43

What would a person of ordinary skill in the 11:43
art understand the word "load" to mean in the context 11:43
of a memory module that's connected to a memory 11:43
controller of a computer system? 11:43
A Just -- you just know it's a memory module 11:43
and that there is load. There are multiple meanings. 11:43
The load could be capacitive load, and the load could 11:43
be also a current load. 11:44
Q Okay. But the memory devices -- I'm sorry. 11:44
Let me withdraw. 11:44
And I'll ask: The memory controller will 11:44
experience some sort of load as the result of the 11:44
memory devices that are on the memory module; right? 11:44
A That's correct. 11:44
Q For example, during a write operation, the 11:44
memory controller will see the load of all of the 11:44
memory devices that are on the memory module, right, 11:44
in the absence of some sort of buffer? 11:44
A I -- I can't agree with that. I mean, it 11:44
would -- you said all the memory devices that are on 11:44
the buffer -- I -- I -- repeat your question. 11:44
Q Sure. 11:44
The question is: During a write operation -- 11:44
well, let me just withdraw. 11:44
And I'll ask: During a write operation, what 11:44

load will the memory controller experience? 11:45
MR. RUECKHEIM: Object to the form. 11:45
THE WITNESS: The -- I -- I can't answer that 11:45
without knowing the way the memory controller is wired 11:45
to the various receivers. I -- I can't answer it 11:45
because I don't know anything about the structure of 11:45
the interconnect. 11:45
MR. TEZYAN: Okay. 11:45
Q But the memory controller during a write 11:45
operation will at least experience some load as a 11:45
result of -- or -- sorry. Let me withdraw the 11:45
question. 11:45
The memory controller during a write 11:45
operation will experience at least some load due to 11:45
the memory devices; is that fair? 11:45
A You know, it depends on the context. 11:45
And the issue is, if it's capacitive load 11:45
you're talking about, it may not matter about the 11:45
memory devices, per se. It's the path that's taken by 11:45
the signal. 11:46
If it's current load that you're talking 11:46
about, then it does depend on the memory device that 11:46
receives the current. 11:46
So I can't answer your question as asked. 11:46
Q Okay. So you say for capacitive load, it may 11:46

depend on the path that's taken by the signal. 11:46
What do you mean by that? 11:46
A The memory controller -- let's take one 11:46
driver. Okay. The driver is connected to the memory 11:46
through metal, usually on a chip itself. There may be 11:46
other ways of making the connection. 11:46
All of those things that are connected to the 11:46
driver have capacitance with respect to ground or with 11:46
respect to the surroundings. 11:46
What I mean by the driver has to drive that 11:46
capacitive load, I mean that if you start with the 11:47
conductor at 0 volts, and you're trying to raise it to 11:47
a higher voltage, you have to charge that inductor. 11:47
And it doesn't matter if the inductor is tied to the 11:47
memory cell end or if it's a stub or where it goes. 11:47
It starts at 0 volts. You have to charge the entire 11:47
conductor. 11:47
That's what I mean. 11:47
Q Okay. So let's assume we have a memory 11:47
module that has four memory devices on it. Okay. 11:48
Then during a write operation, does the 11:48
memory controller see the load of all four of those 11:48
memory devices? 11:48
A It depends how you wire it, but the answer 11:48
could be yes. 11:48

Q Why does it depend how you wire it? 11:48
A Well, okay. Let's suppose that one of those 11:48
four devices is active. Okay. And the other three 11:48
devices are inactive. Okay. 11:48
The inactive device has a load. It may be 11:48
infinite; it may be some small resistance. Okay. 11:48
Whatever it is, it's a load. 11:48
A transmission wave comes down, and it 11:48
touches all four devices if they're connected, even 11:48
though only three are going to respond. That 11:48
transmission wave will bounce back from all of those 11:49
devices, and then it will be reflected back again, 11:49
back and forth and back and forth and back and forth, 11:49
until it dies out. 11:49
What will happen is that the device that you 11:49
want to send the wave will see noise in the terms of 11:49
the reflections. 11:49
Now, if you take those three devices off the 11:49
transmission line and don't have them connected at 11:49
all, if they're gone, the receiving device will see a 11:49
different signal. 11:49
So the -- even though the devices aren't 11:49
going to respond, they load the transmission line. 11:49
Q Understood. 11:49
So how would you take those three devices off 11:49

Q Well, say those signal reflections weren't 11:51
there. Would there be less noise? 11:51
A The -- you can't get around that. They're 11:51
going to -- this is physics. There will be 11:51
reflection. 11:51
Q I'm saying if -- if those inactive devices 11:51
aren't -- aren't there. 11:51
A You'll still see reflections, but not from 11:51
them. 11:51
Q Okay. 11:51
A Can we go to my vitae? 11:51
Q What's that? 11:51
We can return to that at a later time. 11:51
Sorry. I'm -- 11:51
A Okay. 11:51
Q -- on the particular line of questioning I'd 11:51
like to finish. Okay. 11:51
And in your declaration, paragraph 25, you 11:52
also note that a person of skill in the art would have 11:52
been familiar with industry standards such as JEDEC 11:52
and particular DRAM standards, I take it; is that 11:52
fair? 11:52
A Let me see. 11:52
You quoted that -- either you quoted it 11:52
exactly or you got the intent of it. It's fair. 11:52

of the transmission line? 11:49
A I was just giving an example. Okay. You 11:49
might not wire them on a transmission line. I was 11:49
trying to tell you the effect of having these devices 11:50
that aren't going to respond to the signal be part of 11:50
the load. I just gave you the example. Okay. 11:50
I would like you to -- to bring up my 11:50
curriculum vitae. It's at the end of my -- my report. 11:50
Go ahead. My report is up now; isn't it? 11:50
Q We can return to that in a moment, Dr. Stone. 11:50
I'm just trying to understand something here. 11:50
So in the absence of those reflections on the 11:50
signal line from the three inactive memory devices, is 11:50
the signal integrity of the signal to the active 11:50
memory device higher? 11:50
MR. RUECKHEIM: Object to the form. 11:50
THE WITNESS: I -- I -- I'm sorry. The -- I 11:50
didn't talk about integrity. I don't know what you 11:50
mean by "integrity." 11:50
I'm telling you that the reflections will 11:50
cause noise. The noise will be different if you have 11:50
devices on the line that aren't responding. Or if you 11:50
don't have the devices on the line at all, you will 11:51
see different noise. 11:51
MR. TEZYAN: Okay. 11:51

Q Okay. And DRAM devices can be organized in 11:53
what JEDEC calls ranks; right? 11:53
A G -- what does JEDEC call it? 11:53
Q Let me rephrase the question. 11:53
Memory devices can be grouped in what are 11:53
called ranks; right? 11:53
And specifically, DRAM devices can be grouped 11:53
in ranks; is that fair? 11:53
MR. RUECKHEIM: Object to the form. 11:53
THE WITNESS: Yeah, the -- ranks do refer to 11:53
structures com- -- comprising DRAMs. 11:53
MR. TEZYAN: Okay. 11:53
Q You're familiar with the term "rank"; right? 11:53
A I am familiar with the term. 11:53
Q Okay. Have you ever heard the term "rank" 11:53
used to refer to NAND memory? 11:53
MR. RUECKHEIM: Object to the form. 11:53
THE WITNESS: I built such a memory. The 11:53
answer is yes. 11:54
MR. TEZYAN: Q. But did you specifically 11:54
refer to the NAND devices there as ranks of NAND 11:54
devices? 11:54
A Let me give you a citation. I don't have it 11:54
in front of me. But the answer is, it would be in 11:54
that citation. If we may pull up my vitae. It's -- 11:54

it's actually in my declaration. I'll show you the reference. 11:54
Q Okay. Let me know. 11:54
A So okay. Okay. 11:54
In my vitae on page 8, which is PDF file -- this is my declaration. It's 36 of the PDF file. 11:55
Q Uh-huh. 11:55
A Okay. And particularly, I'm looking at reference 4, a book I wrote called "Microcomputer Interfacing." In that book, it shows the structure of a memory system and has four ranks. I don't recall if I called them ranks. A structure is what people would call a rank today. 11:55 11:56
Q And why is that? 11:56
MR. RUECKHEIM: Object to the form. 11:56
MR. TEZYAN: Let me rephrase the question. 11:56
Q Why would the structure of what you say is in the "Microcomputer Interfacing" book be commonly -- I'm sorry. Let me just -- bad question. 11:56
Okay. What is the structure of a rank? 11:56
MR. RUECKHEIM: Object to the form. 11:56
THE WITNESS: Well, let me just say, I'll -- I'll describe what's there and how it relates to the JEDEC standard. 11:56
There's 32 memory cells -- memory chips. 11:56

They're arranged in four rows. Each row responds by writing 8 bits or producing 8 bits on a read command. Each row is separately enabled when they're active. 11:56 11:56 11:57
Now, if we bring up the JEDEC standard, you'll see that the JEDEC DIMMS behave similarly. 11:57 11:57
And if you get to places where people describe ranks, a person of ordinary -- ordinary skill in the art would look at this -- at my -- my design and say, "That's four ranks." And they look at JEDEC and they say, "Yes, those are ranks," regardless of whether the text says it's a rank or not, because that is the view that a person of ordinary skill in the art would have when you align four rows of eight chips each, and you enable one row at a time. That's what a person of ordinary skill would call a rank. 11:57 11:57 11:57 11:57 11:57 11:57 11:57 11:57 11:57
MR. TEZYAN: Q. So regardless of the type of memory that's being used, as long as there are multiple chips in a row, and you can enable one row at a time, that's a rank? 11:57 11:58 11:58
MR. RUECKHEIM: Object to the form. 11:58
THE WITNESS: It's my testimony that a person of ordinary skill would call that a rank in my book. 11:58 11:58
MR. TEZYAN: Q. Are you familiar with what a chip select signal is? 11:58 11:58
A Can you repeat your question? 11:58

Q Sure. 11:58
Are you familiar with what a chip select signal is? 11:58 11:58
A I am. 11:58
Q What is a chip select signal? 11:58
A Again, this depends on the context, and the context has varied in time. 11:58 11:58
Generally, a chip select signal is a signal that enables a chip to react. In various implementations, a chip select signal would be sent on a bus from a controller. Subsequently, chip selects might not be produced on a bus, and they might be produced locally in other ways, and they may be given other names. 11:58 11:58 11:59 11:59 11:59 11:59
But the whole idea of a chip select is when it's present, it says, "I am selecting you." Some devices may require two, both present. But basically, the idea is, "I want you to act." And if it's not active, it says, "I don't want you to act." That's the idea. 11:59 11:59 11:59 11:59 11:59
Q Are chip select signals unique to DRAM? 11:59
A No. 11:59
Q Chip select signals are used in other applications as well? 11:59 11:59
A I have chip selects in my book, and it's 12:00

dated 1982. 12:00
Q Do you recall when DRAM first came out? 12:00
A I -- I -- I can't give you the exact year. 12:00
But in my book, I describe both SRAM, which is static RAM, which requires constant -- constant voltage to maintain the -- the state, and it also describes DRAM, which requires refresh to maintain the state. And that was 1982. It describes the static RAM has chip select and DRAM has chip select. So sometime prior to 1982, you could get to DRAM. I don't know when. 12:00 12:00 12:01 12:01 12:01 12:01 12:01 12:01 12:01
Q Okay. And you're familiar with the structure of DRAM; right? 12:01 12:01
A I don't believe there is a unique structure of DRAM. 12:01 12:01
Q Well, DRAM is comprised of memory cells; right? 12:01 12:01
A The -- I'm -- I'm sorry. The original patent on DRAM are -- I'm sorry. The original patent on the -- on the DRAM cells we use was done at IBM, and it's called a one-cell memory. And if you're talking about, is that DRAM, the answer is yes. 12:02 12:02 12:02 12:02 12:02
And it's a -- I'm sorry. It's a one-transistor cell. And so there's no plural. And you asked your question in the plural. That's what's 12:02 12:02 12:02

confusing to me. 12:02
Q Okay. But a person of ordinary skill in the 12:02
art, when hearing the term "DRAM," would understand 12:02
that DRAM has memory cells; correct? 12:02
MR. RUECKHEIM: Object to the form. 12:02
THE WITNESS: The person -- I think I have to 12:02
go to the context on this. 12:03
Again, you used plural, and I -- it's -- is 12:03
that correct? You said "memory cells"? 12:03
MR. TEZYAN: Yes. 12:03
Q The question was, would a person of 12:03
ordinary -- 12:03
A Yeah, that -- that's what bothers me. So I 12:03
don't know. 12:03
Q Okay. Aside from that implementation at IBM 12:03
that you just discussed, are you aware of any other 12:03
DRAM that's composed of just one memory cell? 12:03
A Well, yes, I am, because FPGAs can be 12:03
configured into one memory cell on an FPA -- FPGA, for 12:03
example. So it wouldn't be in the plural. 12:03
So no, I -- I still have difficulty with your 12:03
question. 12:03
Q Okay. So DRAM that would go inside a memory 12:03
product is composed of DRAM cells; right? 12:04
MR. RUECKHEIM: Object to the form. 12:04

THE WITNESS: I would say the way you're 12:04
offering that is if every instance is composed of 12:04
memory cells. 12:04
And I would say that it is the case that DRAM 12:04
that goes into products in some cases, and maybe in 12:04
many cases, has memory cells. I am not testifying 12:04
that in every case, a DRAM that goes into a memory 12:04
product has memory cells. 12:04
MR. TEZYAN: Q. What would the memory be 12:04
composed of in a DRAM product otherwise? 12:04
MR. RUECKHEIM: Object to the form. 12:04
THE WITNESS: Flip-flops. They not -- 12:04
they're not necessarily called memory cells; they're 12:05
flip-flops. 12:05
MR. TEZYAN: Okay. 12:05
Q So is it your testimony today that a DRAM die 12:05
that goes into a memory product has no DRAM cells in 12:05
it? 12:05
A I didn't testify to that. 12:05
Q Well, it sounds like you're saying that there 12:05
can be DRAM that goes into DRAM products that is not 12:05
composed of memory cells -- DRAM memory cells. 12:05
MR. RUECKHEIM: Object to the form. 12:05
THE WITNESS: I think you asked me that in 12:05
every case, is a DRAM product that goes into a -- I'm 12:05

sorry -- that a DRAM that goes into a product composed 12:05
of memory cells? 12:06
And I said there are -- there are situations 12:06
and possibly not. And then I gave an example which 12:06
are the registers, which you don't call memory cells. 12:06
And -- okay. I can conceive of an FPGA going 12:06
into a product, and that FPGA has registers in it, 12:06
flip-flops, if you'd like, and they -- they do 12:06
something. And you might not call them memory cells 12:06
because they're not -- they're not compatible with 12:06
JEDEC. All right. So I -- that's -- that's a 12:06
possible way to interpret your question. 12:06
And my answer would be yes, these things 12:06
would not be DRAM -- necessarily DRAM memory. 12:06
MR. TEZYAN: Okay. 12:06
Q Let's go back to paragraph 25 of your 12:06
declaration where you discuss -- or where you note 12:06
that a person of ordinary skill in the art would have 12:07
been familiar with standardized DRAM memory devices; 12:07
fair? 12:07
That's what it says there? 12:07
A Yes. 12:07
Q Okay. And those DRAM memory devices would 12:07
have DRAM memory cells; right? 12:07
MR. RUECKHEIM: Object to the form. 12:07

THE WITNESS: Okay. The answer is, if you -- 12:07
if you're insisting that every instance would have 12:07
memory cells, I don't know. 12:07
If you're insisting that in -- in many cases 12:07
or in some instances or whatever, those DRAM devices 12:07
would have memory cells, my answer is yes. 12:07
I'm just not able to say in every possible 12:07
case. 12:08
MR. TEZYAN: Q. Would a person of ordinary 12:08
skill in the art at the time of these patents have 12:08
been aware of JEDEC standardized memory devices that 12:08
were 64 bits wide? 12:08
A I'd have to check on the dates of the JEDEC 12:08
standards. I'm not exactly sure when the 64-bit-wide 12:08
JEDEC module was introduced. I believe that the DDR2 12:08
predates the priority of the '918 patent. So I'd have 12:08
to look at the DDR2 and see what width it has. 12:09
Q Let me clarify my question a little bit. I 12:09
meant 64-bit memory devices; so not the memory module 12:09
itself, but the SDRAMs that are on the module. 12:09
Would a person of ordinary skill in the art 12:09
been aware of such memory devices? 12:09
A I don't know when they were introduced. I 12:09
didn't prepare for that. 12:09
Q But you're referring to the memory module, 12:09

right, not the individual SDRAMs, the chips? 12:09
A My answer was for the memory module. I 12:09
didn't mention any JEDEC DDR2 standard. 12:09
Q Right. 12:09
And my question is: Are you aware of any 12:09
SDRAM chips that are 64 bits wide? 12:09
A I -- I don't know when they were first 12:09
introduced. I can't -- I can't testify on that. 12:09
MR. TEZYAN: Okay. It's 12:10. Why don't we 12:10
take a break for lunch, since it's around lunchtime on 12:10
the West Coast. 12:10
THE VIDEOGRAPHER: All right. 12:10
MR. TEZYAN: Go off the record. 12:10
THE VIDEOGRAPHER: We'll go off the record. 12:10
The time is 12:10 p.m. 12:10
And it's the end of Media No. 4. 12:10
(Lunch break taken at 12:10 p.m.) 12:10
---oOo---

That's an electronic version of a book I wrote that 13:03
has the publication date of 1982. 13:03
Q And this was the book that you had referenced 13:03
earlier when I asked you for an example of using the 13:03
term "rank" with reference to NAND memory; is that 13:03
right? 13:03
A That's correct. 13:03
Q Can you show me where in this book that 13:03
example is? 13:03
A I can show you. And I will tell you in 13:03
advance that it uses the word "bank" instead of 13:03
"rank," but let me find it for you. 13:03
The figure that I have in mind appears on 13:03
page 146 of the PDF file. 13:04
Q Okay. And that's Figure 4-5; correct? 13:04
A That's correct. 13:04
Now, the use of the term "bank" -- let's see. 13:04
I'll take a moment. 13:04
Q Take your time. 13:04
A Look on page 145 of the PDF file, and the 13:04
first line is part of a sentence. In the middle of 13:05
the sentence, it says: 13:05
"Control signals are passed parallel to a 13:05
bank of eight chips." 13:05
And that's just before Figure 4.4. 13:05

A F T E R N O O N S E S S I O N
June 26, 2023 1:00 P.M.
---oOo---

THE VIDEOGRAPHER: We're going back on the 13:02
record. The time is 1:02 p.m. 13:02
And this is the start of Media Unit No. 5. 13:02
MR. TEZYAN: Welcome back, Dr. Stone. 13:02
Q Did you have any communications with counsel 13:02
on the break? 13:02
A I did not. 13:02
Q Before the break, you had mentioned one of 13:02
your books. I believe it's the micro interfacing -- 13:02
I'm sorry. I butchered the title of that book. But 13:02
I've uploaded it as Exhibit 8. 13:02
(Document remotely marked Exhibit 8 13:02
for identification.) 13:02
MR. TEZYAN: Q. Can you please update your 13:02
Exhibit Share? 13:02
A Sure. I have downloaded it already. 13:02
Q Fantastic. 13:02
What is Exhibit 8? 13:02
A I'm sorry. Repeat your question, please. 13:02
Q What is Exhibit 8? 13:02
A Exhibit 8 is "Microcomputer Interfacing." 13:02

Q Okay. But a person of ordinary skill in the 13:05
art in, let's say, 2006 would have understood the 13:05
terms "bank" and "rank" to be referring to different 13:05
things; right? 13:05
MR. RUECKHEIM: Object to the form; beyond 13:05
the scope. 13:05
THE WITNESS: I believe that the difference 13:05
between "bank" and "rank" would vary with the -- would 13:05
vary with the person of ordinary skill. I believe 13:06
that Figure 4.5 that I call banks would be viewed as 13:06
ranks as well by a person of ordinary skill in the 13:06
art. 13:06
MR. TEZYAN: Q. And why is that, sir? 13:06
A Well -- 13:06
MR. RUECKHEIM: Same objections. 13:06
THE WITNESS: -- the bus that connects the 13:06
data -- I'm sorry. 13:06
The chip select that goes out to the eight 13:06
chips, you use a different chip select for each of the 13:06
eight -- this is -- I'm sorry. 16 columns. It's 13:06
16 columns by eight rows. So we have 16 chip selects. 13:06
And the person of ordinary skill would say, 13:07
"Well, I'm either going to select bank 0 or bank 15." 13:07
And that person of ordinary skill could say, "Well, 13:07
these are ranks, rank 0 to rank 15." 13:07

That's because there was no firm definition of what a bank and a rank was in those days.
MR. TEZYAN: Okay.
Q But at some point, the use of the word "rank" became standard to differentiate it from a "bank"; right?
MR. RUECKHEIM: Same objections.
THE WITNESS: I don't know if it became standard. I know that rank is used today, and I know there was a time when rank and bank were both used. And at the time I wrote this, bank was.
But look at the structure. Okay. So the structure is telling.
MR. TEZYAN: Q. Were you done with your answer?
A I'm done with my answer.
Is that what you're asking?
Q Yeah.
Okay. So let me clarify something you said a little bit earlier. You testified that chip selects might not be produced on a bus, and they might be produced locally in other ways.
Do you recall that testimony?
A I do.
MR. RUECKHEIM: Object to the form.

MR. TEZYAN: Okay.
Q What did you mean by that?
A Well, in this example, the chip select is produced locally. It's --
Q What does -- sorry.
A I'm sorry?
Q I was going to ask: What do you mean by it might be "produced locally"?
A Do you see that 4-by-16 decoder?
Q Yes.
A 4 bits from -- I'm sorry -- 4 bits from the address go to the decoder, and they're used in this case, in this example, to create chip selects. 4 bits give you 16 possibilities, and that's how we select them. In that case, I would say this chip select is produced on the board. It's produced locally.
If you want to say -- give an example of something where it's not produced locally, the chip select could be produced on the memory bus by a controller. And the controller may be two, three -- I'm sorry -- two or four chip selects, for example. And the controller can select a bank or a rank by enabling one of the four or one of the two chip selects. In that case, the controller would produce the chip select. And I would say it's not produced on

the board, so it would not be produced locally.
Q Understood.
So when you say that the chip select might be produced locally, in other words, what you're saying is it might be produced on the memory module; right?
A In this example, yes.
Q Okay. Is another example of that when the memory controller transmits packetized information to the memory module that's then also decoded on the memory module to produce chip select signals?
MR. RUECKHEIM: Object to the form; beyond the scope.
THE WITNESS: Your hypothetical may have many answers. I would have to -- to ask you more about all of the parameters in that. So it's -- it's too complicated for me to answer directly. I -- I think that's what my testimony is right now.
MR. TEZYAN: Okay.
Q In this example, you have multiple memory devices for each rank; is that correct?
In other words, how many ranks are on this memory device depicted here?
A The chip select can select among 16 banks or ranks. So there's 16 banks or ranks. Each bank or rank comprises eight chips. That's my answer.

Q Okay. So the answer to my question is yes, there are multiple devices for each of the ranks depicted here; is that correct?
A There are multiple devices on each of the banks or ranks, yes.
Q Okay. So a person of ordinary skill in the art would not refer to a single memory device as a rank; fair?
MR. RUECKHEIM: Object to the form, and beyond the scope.
THE WITNESS: The answer is no. I don't believe that's a fair answer.
MR. RUECKHEIM: And Counsel, you're getting -- straying well outside his report. Do these questions relate at all to the claim construction declaration that the deposition is supposed to be directed to?
MR. TEZYAN: Q. Dr. Stone, can you pull up the '918 patent?
A Would you repeat your question.
Q I'm sorry. Could you please pull up the '918 patent.
A Okay. I'm pulling up Exhibit 4.
I have it.
Q And could you go to Claim No. 12, please. I

believe that's on page 47. 13:13
A I have it. 13:13
Q Okay. So Claim No. 12 is a dependent claim 13:13
from Claim 5; right? 13:13
A That's correct. 13:13
Q And it recites: 13:13
"The plurality of components further 13:13
comprising: a non-volatile memory." 13:13
Right? 13:13
A That's correct. 13:13
Q And a controller that's: 13:13
"Configured to receive the trigger signal, 13:13
wherein, in response to the trigger signal, the 13:13
controller performs a write operation to the 13:14
non-volatile memory." 13:14
Right? 13:14
A That's correct. 13:14
Q So the controller needs to be connected to 13:14
the non-volatile memory; fair? 13:14
MR. RUECKHEIM: Object to the form. 13:14
THE WITNESS: I'm not sure what you mean by 13:14
"connected." The controller has to control the 13:14
non-volatile memory. 13:14
MR. TEZYAN: Right. 13:14
Q But here specifically, it says: 13:14

"The controller performs a write operation to 13:14
the non-volatile memory." 13:14
Right? 13:14
A It -- the: 13:14
"The controller performs a write operation to 13:14
the non-volatile memory." 13:14
That's correct. 13:14
Q Okay. So would a person of ordinary skill in 13:14
the art understand that the controller needs to be 13:14
connected to the non-volatile memory? 13:14
MR. RUECKHEIM: Object to the form. 13:14
THE WITNESS: Yeah, the -- your use of the 13:14
word "connected" can be interpreted many different 13:14
ways. So I don't know how to answer the question 13:14
unless you tell me specifically what you mean by 13:14
"connected." 13:15
MR. TEZYAN: Q. What does the word 13:15
"connected to" mean to you? 13:15
A Well, it could be attached directly to, or it 13:15
may be that the controller goes -- sends an operation 13:15
request to an intermediate device, and that sends it 13:15
on to another intermediate device, and that goes to 13:15
the non-volatile memory. 13:15
So I'm not sure what question I'm answering 13:15
if I say "yes" or "no." 13:15

Q Would your answer change depending on those 13:15
definitions? 13:16
MR. RUECKHEIM: Object to the form. 13:16
THE WITNESS: If you had a situation in which 13:16
the controller is connected to the non-volatile memory 13:16
through intermediate devices, and you're using the 13:16
connected through intermediate devices as if it 13:16
meant -- as -- I'm sorry. 13:16
If I'm answering, "No, because there's 13:16
intermediate devices," and you would say, "No, it's 13:16
really connected," then we are at odds. 13:16
And conversely, if it's directly connected, I 13:16
would -- I would say it's connected then one way or 13:16
the other. 13:16
But we -- we could come up with different 13:16
answers, "yes" and "no," depending on how we interpret 13:16
indirect connection. That's the issue. 13:16
MR. TEZYAN: Okay. 13:16
Q Is the controller not connected to the 13:16
non-volatile memory if there is an intermediary in 13:16
between? 13:16
MR. RUECKHEIM: Object to the form. 13:16
THE WITNESS: Again, you used the word 13:17
"connected." 13:17
MR. TEZYAN: Yeah, and I'll just repeat the 13:17

question. 13:17
Q Is the controller not connected to the 13:17
non-volatile memory if there is an intermediary in 13:17
between? 13:17
MR. RUECKHEIM: Same objection. 13:17
THE WITNESS: You're -- I -- I need to know 13:17
what you mean when you say is connected or not 13:17
connected. If there's intermediate devices between, 13:17
that's -- that says something. Now, you tell me what 13:17
you mean by "connected." 13:17
MR. TEZYAN: Okay. 13:17
Q I think we can agree that if connected means 13:17
attached to, right, that the non-volatile memory -- 13:17
I'm sorry. Let me back up. 13:17
Okay. So you're saying "connected to" could 13:17
mean either attached directly or attached to an 13:17
intermediary; correct? 13:17
A At least those two, yes. 13:17
Q Okay. So my question is -- is really: In 13:17
the case where you're saying the controller and 13:17
non-volatile memory are indirectly connected, that's 13:18
not a connection? 13:18
MR. RUECKHEIM: Object to the form. 13:18
THE WITNESS: No. 13:18
The -- you're still using the word 13:18

"connection," and I don't know how you mean. And so I can't answer until you -- you need to define "connected," and then I can handle it.

MR. TEZYAN: Okay.

Q Well, you provided me two definitions of "connection." And I'm just asking you to apply the second one and answer whether, under those circumstances, you think that the non-volatile memory and the controller would need to be connected?

A And --

MR. RUECKHEIM: Object to the form.

THE WITNESS: -- the second definition was the controller -- "connection" can mean indirectly with intermediate devices; is that correct?

MR. TEZYAN: Yes.

THE WITNESS: If the controller is attached to the non-volatile memory through intermediate devices, using your second definition of connection that allows that connection to have intermediate devices, then the controller is connected to non-volatile memory with your definition.

MR. TEZYAN: Okay.

Q And if we define "connected to" to mean "attached to," that would also be a connection; right?

MR. RUECKHEIM: Object to the form.

THE WITNESS: I want to ascertain that "attached to" means directly, without intervening -- intervening devices.

The fact is if there are inter- -- intervening devices, you should know about that. And if there are not, you should also know about that. So the --

MR. TEZYAN: That's -- that's fair.

Q So assume there's no intermediary devices. In that situation, is the controller and non-volatile memory connected?

A Using the first --

MR. RUECKHEIM: Objection.

THE WITNESS: -- definition -- is that the definition you want me to use?

MR. TEZYAN: Yes.

THE WITNESS: In that case, the controller is connected to the non-volatile memory, because your first definition of "connection" means that there are no intermediate devices.

MR. TEZYAN: Okay.

Q So under either definition of "connected to," is it fair that in order to perform a write operation to non-volatile memory, the controller has to be connected to non-volatile memory?

MR. RUECKHEIM: Object to the form.

MR. TEZYAN: Q. Either through an intermediary or directly?

A Got it.

So the controller needs to be connected directly or indirectly to the non-volatile memory in order to perform the write operation in the non-volatile memory. That is my testimony.

(Document remotely marked Exhibit 9 for identification.)

MR. TEZYAN: I've gone ahead and produced Exhibit 9.

Q Could you please refresh your Exhibit Share and download Exhibit 9 when it comes up.

A Okay. I'm downloading it now.

Okay. I have it downloaded. Now I'll bring it up.

I have it.

Q What is Exhibit 9, Dr. Stone?

A This is the '060 patent.

Q Could you please go to Figure 1A.

A Okay.

Q And if you need to rotate your screen, that's fine.

A Okay. I -- I just rotated it. Go ahead.

Q Okay. So the rectangles that are annotated 110, those are the array dies; correct?

A Yes, those are dies.

Q And specifically, the array dies that the patent talks about; right?

A They're -- they are the array dies. That's correct.

Q Okay. And the vertical line that's labeled 120, that's the die interconnect; right?

A That's the die interconnect. That's correct.

Q And 134 is a data driver; correct?

A That's correct.

Q So does what's depicted in Figure 1A correspond to a multi-drop configuration?

A I can't tell.

Q Are you familiar with the term "multi-drop" --

A I am.

Q -- like if you're referring to a multi-drop TSV configuration?

A Well, I -- there is not sufficient detail. But I will tell you what would make it multi-drop if I had the detail.

Q Okay.

A Okay. 144, those three lines attached from

the driver -- the driver level to three different 13:24
dies, I can't tell what's on those dies. If those 13:24
dies each had something to connect to, you could -- 13:24
and let's say the first -- the shortest 144 connected 13:25
to it sometimes, and the second 144 connected to it 13:25
sometimes, and the third connected to it sometimes. 13:25
You might consider that multi-drop if all three 144 13:25
lines were connected. 13:25
Q Fair enough. 13:25
But my question was specific to the -- the 13:25
data die interconnect. Right. 13:25
If -- if you want to refresh your memory, in 13:25
column 1, lines, I think, 39 through about 46, it 13:25
states that the -- let's see -- the driver 140 is for 13:25
command and address signals. And 144, those are chip 13:26
select lines; right? 13:26
A That's correct. 144 are chip selects. 13:26
That's correct. 13:26
Q Yeah. 13:26
And 142 are command and address signals; 13:26
right? 13:26
A That's correct. 13:26
Q Okay. So specifically for the data signals 13:26
on the die interconnect that's for data connected to 13:26
driver 134, is that in a multi-drop arrangement? 13:26

A I can't tell from the figure. 13:26
Q Why not? 13:26
A I don't know what is driving on the dies. 13:26
Q Oh, what do you mean by that? 13:26
A Well, let me get the figure up again. Just a 13:26
second. 13:26
So 134 comes out of a driver and goes up to 13:27
three different levels of the die; is that correct? 13:27
Q Yes. 13:27
A If nothing was connected at the first and 13:27
second level, but only the third level, it would not 13:27
be multi-drop. And I can't tell. 13:27
Q What do you mean by nothing is connected? If 13:27
there is no driver or receiver pair on that die? 13:27
A This VIA can be connected to a die or not 13:27
connected to a die. I mean, if the VIA is not 13:27
connected to the die, and there's nothing for it to 13:27
connect to, then if the first and second ones are not 13:27
connected to the die at all, and the third one is, 13:27
that's not multi-drop. 13:27
Q Okay. Let's take a look at paragraph 29 of 13:28
your declaration, and that's on PDF page 12. 13:28
A Just a moment. I'm going to pull it up from 13:28
what I downloaded just to make sure I've got exactly 13:28
the same thing that you have. 13:28

My declaration is Exhibit 1. 13:28
Q Correct. 13:28
A I'm pulling up Exhibit 1. 13:28
And you want me to go to paragraph -- 13:28
Q Paragraph 29. 13:28
A -- 29? 13:28
Q Uh-huh. 13:28
A I'm there. 13:28
Q And you see this annotated version of 13:28
Figure 1B here; right? 13:28
A I see, yes. 13:28
Q And there is a green line that indicates the 13:29
data die interconnect 182; right? 13:29
A I do. 13:29
Q Okay. That die interconnect is in electrical 13:29
communication with each of these array dies; right? 13:29
MR. RUECKHEIM: Object to the form. 13:29
THE WITNESS: I'm looking where it says that 13:29
in my report. I -- I see. It -- it says: 13:29
"That ... [includes] a driver 184 that drives 13:29
data signals to each of the array dies 160." 13:29
Okay. I see that. 13:29
MR. TEZYAN: Q. And just so I'm clear, I 13:29
asked: That die interconnect is in electrical 13:29
communication with each of those array dies; right? 13:29

A And I -- you're -- you're using "electrical 13:30
communication" as the patent teaches? 13:30
Q Yes. 13:30
A And they're attached -- yes. I would say 13:30
yes, it's in electrical communication with each of 13:30
those array dies. 13:30
Q Okay. So going back to my earlier questions 13:30
then, does this correspond to a multi-drop 13:30
configuration? 13:30
A I -- I don't have sufficient information. 13:30
MR. TEZYAN: Let me pull up an example. One 13:30
moment. 13:30
(Document remotely marked Exhibit 10 13:31
for identification.) 13:31
MR. TEZYAN: Q. Please refresh your Exhibit 13:31
Share. 13:31
A Okay. 13:31
Q Let me know when you have the latest exhibit. 13:31
A I'm just starting to load Exhibit 10, and 13:32
I'll be downloading it. 13:32
I have downloaded Exhibit 10. 13:32
Q Okay. Exhibit 10 is an ISSCC paper entitled: 13:32
"A 1.2V 64Gb 341GB/s HBM2 Stacked DRAM with 13:32
Spiral Point-to-Point TSV Structure and Improved Bank 13:32
Group Data Control." 13:32

Right? 13:32
A Yes, that's the title. 13:32
Q Okay. Feel free to look it over if you'd 13:32
like to. But my questions are about Figure 12.3.1 13:32
that appears on page 2. So let me know when you're 13:32
there. 13:32
A Okay. I will have difficulty making 13:33
testimony on this because I've just seen it for the 13:33
first time. I'll do my best. But I may just say I 13:33
need time to read it, and read it carefully. 13:33
Let me take a look. 13:33
Q That's fine. Take as much time as you need. 13:33
A Well, I'm ready to attempt an answer, but 13:34
I -- I believe that I really need a lot of time to 13:34
read this. Go ahead and ask your question. 13:34
Q That's fair. 13:34
My question is just very discrete here. So 13:34
on page 2, Figure 12.3.1, you see a figure that 13:34
underneath says "Conventional Multi-Drop"; right? 13:34
A Yes. 13:34
Q So when I'm using the word "multi-drop" in my 13:34
previous questions, I'm referring to this sort of an 13:35
arrangement. 13:35
Is that making sense, where the TSVs -- 13:35
A I understand. I understand. 13:35

Q -- where the TSVs that are connected to 13:35
channel 0 are connected to the drivers on each of the 13:35
die? 13:35
A Yes, I understand that. 13:35
Q Okay. So going back to Figure 1A of the 13:35
'060 patent, is it still the case that you can't tell 13:35
from the figure alone whether this depicts a 13:35
multi-drop configuration? 13:35
A That's correct. 13:35
Q Okay. And why is that? 13:35
A Figure -- that figure doesn't show whether 13:35
the VIA on any die is connected to a data port. You 13:35
can be connected to the die but not to a data port, or 13:35
you could be connected to a die and you're connected 13:35
to a data port. So I can't tell. 13:35
Q Okay. But if you're not connected to a data 13:36
port, there is no electrical communication to the die; 13:36
right? 13:36
A That's false. That's false. 13:36
MR. RUECKHEIM: Objection. 13:36
MR. TEZYAN: Okay. 13:36
Q Why is that? 13:36
A I would like you to open my book, please. 13:36
Q I'd -- I'd prefer if you just answer my 13:36
question. 13:36

A There's an answer in my book. I have a 13:36
diagram that explains why. 13:36
Q Could you summarize your answer without -- 13:36
A No. I want to see the diagram. 13:36
Q I'd prefer if you'd just give me an answer 13:36
first, sir. 13:36
A I can't do that. I need to show you the 13:36
diagram. 13:36
Q You can't provide me an answer without the 13:36
diagram? 13:36
A I can. 13:36
MR. RUECKHEIM: Objection to form. 13:36
THE WITNESS: It will not be -- it will not 13:36
be informative. I need the diagram. 13:36
MR. TEZYAN: Okay. 13:37
Q Where is -- which exhibit is this? 13:37
A My book is now the Exhibit 8. And -- 13:37
Q Okay. 13:37
A -- in my book, the book page number is 54. 13:37
I'll get you the PDF page number in a minute. The 13:37
material of interest begins on PDF page 54. It's 13:37
called: 13:37
"Transmission-Line Techniques." 13:37
Q I'm sorry. That's internal page number? 13:37
A On the PDF file, it's -- oh, I'm sorry. I -- 13:37

it's 54 in my reader. It may be 69 in your reader. 13:38
Q Okay. I'm there. 13:38
A Okay. It says: 13:38
"Transmission-Line Techniques." 13:38
This tells you how waves flow on 13:38
interconnections. 13:38
I'm going to now go down to a part that shows 13:38
what happens when you connect it to a stub on a die 13:38
interconnect. 13:38
Whoops. Where is it? 13:38
One picture -- oh, let's start on PDF 13:38
page 78. 13:38
Do you see this? 13:38
Q Figure 2.19? 13:38
A 2.19. 13:39
Q Okay. 13:39
A You see all that noise? That noise is 13:39
present because of reflections on the transmission 13:39
line. Okay. 13:39
If you disconnect one of those drivers -- one 13:39
of those receivers, you'll get a different kind of 13:39
noise, but you'll see the noise. That's because the 13:39
wave is an electrical communication with a stub, even 13:39
if there is no port array on it. 13:39
Now, let me go down a little further to show 13:39

you what's happening. Look at Figure 2.20, page 79. 13:39
Okay. On this page, a wave is sent from the left 13:39
where there -- you see the Z0, and it goes out to 13:39
where there's a junction. At the junction, it's 13:39
reflected back, and part of the wave goes forward 13:39
straight; part of it goes to the left. That's what 13:40
you're dealing with with physics. 13:40
And that happens when you're connected to the 13:40
die, regardless of what happens on the die, whether 13:40
there is a port array connected to it or not. 13:40
So what happens is that the wave propagates 13:40
on the die along the stub or to the port array, and it 13:40
bounces back again. So those waves are going back and 13:40
forth and back and forth, and that's what causes the 13:40
noise that you saw in the earlier figure. 13:40
Let me go back to 2.19. Do you see that 13:40
noise there? Each bump or change is a result of a 13:40
reflection, and the reflections come from the port 13:40
arrays, the data arrays on the ports. They also come 13:40
from the stubs if they don't have a data port 13:40
connected, and they come from the points where there's 13:40
a branch. 13:41
So changing things by removing or adding 13:41
devices only changes the noise, unless you don't have 13:41
a multi -- unless there are no stubs or no drivers. 13:41

Then you -- then you can get a predictable wave. And 13:41
that has -- that even has reflections, but it looks 13:41
different. 13:41
So that's my testimony. 13:41
Q Okay. Let me see if I understand something. 13:41
Is it your testimony that the connection 13:41
between a TSV and a stub is electrical communication? 13:41
A Yeah. This demonstrates it, because the wave 13:41
travels on that. 13:41
Q Okay. What does the word "electrical 13:41
communication" mean to you? 13:41
A Electrical connection. That's -- I got that 13:41
from the patent. I can show you where he says that. 13:41
Q Okay. Show me. 13:41
A Okay. The patent -- the -- is what exhibit? 13:41
Q Exhibit 9, sir. 13:42
A Okay. I'll open the Exhibit 9. 13:42
So I have the '060 patent up. I'll -- I will 13:42
find that reference that says that it connects -- 13:42
makes the association between electrical communication 13:43
and electrical connection. 13:43
I would like you to look at column 17. 13:43
Q Okay. I'm there. 13:43
A I'm looking at line 65. Line 65 reads: 13:43
"Forming the electrical connections places 13:43

the die interconnects in" -- "communication with the 13:43
respective drivers." 13:44
Okay. Now, let's see. There may be 13:44
additional I would like to look at. Now, continuing 13:44
on from that point, it says: 13:44
"In some embodiments, forming the electrical 13:44
connections can comprise forming electrical 13:44
connections between the die interconnects and a data 13:44
conduit." 13:44
Okay. 13:44
Q I'm sorry to interrupt, but can I ask a 13:44
clarifying question? 13:44
A And see, that -- that -- well, actually, 13:44
that's not so relevant. It's the previous sentence 13:44
that I read: 13:44
"Forming the electrical connections places 13:44
the die interconnects in electrical communication with 13:44
the respective drivers." 13:44
So what we've done is we -- if you connect a 13:44
die interconnect to a -- one of the levels in the 13:45
figure, you now are connecting to some conductor. 13:45
That conductor will carry a wave when you -- when you 13:45
drive it. It has capacitance. It has a load. 13:45
And whether or not that conductor is -- is 13:45
attached to a data port, you will see the wave go down 13:45

that conductor. At the end, it will bounce -- bounce 13:45
back, and you'll see that as noise. Moreover, the 13:45
capacitance on the conductor will load the driver. 13:45
So in every way, forming the electrical 13:45
connection and placing this piece of a -- of a metal 13:45
on the -- on an array, it will form to an electrical 13:45
communication. That's what you'll get. Electrical 13:45
connection is electrical communication in this sense. 13:45
Q Okay. But can I ask a clarifying question? 13:46
So on line 65, column 17, it says: 13:46
"Forming the electrical connection places the 13:46
die interconnects in electrical communication with the 13:46
respective drivers." 13:46
Right? 13:46
That's talking about the drivers on the 13:46
control die; right? 13:46
A That's correct. 13:46
Q Okay. So it's not talking about electrical 13:46
communication with the array dies; right? 13:46
A No. I disagree. 13:46
Q Why? 13:46
A You -- you will understand that the VIA is 13:46
now connected to the -- to the array die, because 13:46
there may be metal there. There may be a metal -- a 13:46
metal pathway. 13:46

Q I understand. 13:46
But you're saying that this specific 13:46
disclosure that equates electrical connection with 13:46
electrical communication discusses array dies. 13:46
And I'm pointing out to you that it 13:46
specifically says drivers, and these are drivers in 13:46
the control die; right? 13:47
A Yeah, but that's fine. The driver is in 13:47
communication with whatever the -- the VIA is 13:47
connected to on that die. 13:47
Q Does the passage mention electrical 13:47
communication with array dies? 13:47
MR. RUECKHEIM: Object to the form. 13:47
THE WITNESS: Does the -- it just -- it just 13:47
did. That's what it says. 13:47
MR. TEZYAN: Q. Where does it say "array 13:47
die" in this paragraph, sir? 13:47
A Just a moment. 13:47
Okay. There is a reference to this in 13:48
column 8 at line 57. 13:48
Q And I don't mean to cut you off, sir, but the 13:48
question was about paragraph -- the paragraph starting 13:48
on line 60 of column 17. 13:48
And the question was: Where in that 13:48
paragraph that you claim provides support for your 13:48

opinion that the patentee equated electrical 13:48
connection with electrical communication does it talk 13:48
about electrical communication with the array dies 13:48
explicitly? 13:48
A All right. 13:49
I have to add to my opinion the description 13:49
that further clarifies what that sentence means. And 13:51
if you don't mind, I would like to now refer to -- 13:51
MR. TEZYAN: That -- okay. So I'm going to 13:51
move to strike as nonresponsive. 13:51
Q It's specifically the paragraph -- 13:51
A Here is -- 13:51
Q -- in column 17 -- 13:51
A I will amend my response. 13:51
Q I'm sorry. What? 13:51
A Let me amend my response so that it's not 13:51
stricken from the record so I can get it right. 13:51
Q Okay. But can you answer the question first, 13:51
sir? 13:51
The question was specifically -- 13:51
MR. RUECKHEIM: You cut off -- you cut off 13:51
his answer. Can you allow the witness to answer the 13:51
question? 13:51
MR. TEZYAN: He's answering the question he 13:51
wants to answer, and I want him to answer my question. 13:51

MR. RUECKHEIM: You didn't let him give but 13:51
three words. 13:51
THE WITNESS: Okay. 13:51
MR. TEZYAN: Dr. Stone, if I may just 13:51
answer -- ask my question one more time. 13:51
Q So the paragraph starting on line 60 of 13:51
column 17, okay, where in that paragraph that you 13:52
claim provides support for your opinion that 13:52
electrical connection and electrical communication are 13:52
the same does it talk about the array dies? 13:52
A It refers to the process 500. If we look 13:52
back at the process 500, we will understand that the 13:52
process 500 allows you to make a connection between 13:52
the die interconnect and the array die. 13:52
Q Were you done with your answer? 13:52
A That's -- that's -- I would like now to look 13:52
at the description of process 500. May -- I'm going 13:52
to do that. 13:52
Q Okay. 13:52
A Now, on column 17, line 24, the first 13:53
sentence says: 13:53
"The process 500 further comprises forming 13:53
electrical connections between the first die 13:53
interconnect and the first subset of array dies in an 13:53
operational block 504." 13:53

So there is where the connection is made. 13:53
And if you -- if you go on, it tells you that 13:53
at line 29: 13:53
"Forming the electrical connections places 13:53
the die interconnects in electrical communication with 13:53
the respective subsets of array dies." 13:53
Q Okay. Can we go back to Figure 1A? 13:53
A Okay. In this patent? 13:54
Q Yes, sir. 13:54
So in Figure 1A, we have these multiple array 13:54
dies 110; right? 13:54
A I see that. 13:54
Q And they're connected via die 13:54
interconnect 120 to driver 134; right? 13:54
A That's correct. 13:54
Q So can the multiple array dies output data in 13:54
parallel to driver 134? 13:54
MR. RUECKHEIM: Object to the form. 13:54
THE WITNESS: I -- I -- I need you to repeat 13:54
your question. I'm not sure I understand it. 13:54
MR. TEZYAN: Sure. No problem. 13:54
Q So can the multiple array dies output data in 13:54
parallel to the driver? 13:54
A It doesn't say. 13:55
Q Right. 13:55

But would a person of ordinary skill in the art, looking at this, understand that the array dies could do that? 13:55

A It's not specified yes or no. I -- so I'm not sure. There may be some teaching that says yes, some teaching that says no. In isolation, I cannot tell by looking at Figure 1A whether they can output in parallel. 13:55

Q Let me give a more concrete example, maybe. So suppose the -- you have a read operation; right? Can multiple array dies respond to that read operation at the same time? 13:55

MR. RUECKHEIM: Object to the form. 13:55

THE WITNESS: In this diagram? 13:56

MR. TEZYAN: Q. Assuming you had the memory package that's depicted in this diagram, yeah. 13:56

A I can't tell from this diagram alone, no. I don't know. I'd need more information to answer that question. 13:56

Q Well, this diagram depicts that all of the array dies share one die interconnect for the data driver 134; right? 13:56

A In this diagram, there's only one data driver. Yes. 13:56

Q Okay. And so to put my question another way, 13:56

could all of the array dies output data at the same time to that driver 134 along the die interconnect? 13:56

MR. RUECKHEIM: Object to the form. 13:57

THE WITNESS: Are you asking the question that -- here's the hypothesis as I understand it. 13:57

Each of the layers 110 has a memory that somehow or other is triggered to output data. And somehow or other, all the memories on those array levels are triggered at the same time. So all of the cells attempt to output data at the same time. Not only that, they all output onto die interconnect 110. 13:57

You're asking, is this possible? That probably is not possible. It just -- it would be unusual. I can't say it can't happen. But I think that's what you're talking about. 13:57

MR. TEZYAN: Yeah, that sounds about right. 13:57

Q And I guess my question is: Why would that not be possible? 13:57

A Well, I can give you an example where it is possible, and then I can give you an example where it's not possible. 13:58

Q Okay. 13:58

A The example where it is possible is if you output all the things at the same time and do something so that they don't conflict at the die 13:58

interconnect. Not conflicting means that you know they're all going to be 1s, or they're all going to be 0s, or you know that some are disconnected. As long as there are no conflicts at the die interconnect, you may succeed, but you may need to have intervening logic. 13:58

On the other hand, you will probably run into a problem, not necessarily a failure, if one driver on one array layer is driving a 0, and another driver on a different array layer is driving a 1. Now, that does happen. That does happen, okay, and that happens when you're finishing an operation on one, and you're starting an operation on the other. Because of timing, there could be a moment or two, a brief period, when both drivers are active in the opposite direction. And you can design those layers to protect against damage. 13:58

So the answer is, if there are two -- just two layers and they are operated in parallel, the answer is that could happen, yes. 13:59

Q Okay. So if I understand your answer correctly, the reason why it might be a problem is the risk of data collisions; right? 13:59

A That's correct. 14:00

MR. TEZYAN: Okay. I think we can take a 14:00

ten-minute break now if that's fine with you guys. 14:00

THE WITNESS: Okay. Let's do that. 14:00

THE VIDEOGRAPHER: We're going to go off the record. The time is 2:00 p.m. 14:00

And this is the end of Media Unit No. 5. 14:00

(Recess taken.) 14:00

THE VIDEOGRAPHER: We're going back on the record. The time is 2:15 p.m. 14:14

And this is the start of Media Unit No. 6. 14:15

MR. TEZYAN: Q. So you testified that there are certain scenarios where it would be okay for all three of the dies that are depicted in Figure 1A to drive along die interconnect 120. 14:15

Do you recall that testimony? 14:15

A I said there might be. I -- yes, I do recall that. 14:15

Q Okay. And would your answer change if two of the three dies were outputting data at the same time? 14:15

A I -- I'm sorry. I don't have all of the hypotheses in mind. So can you give me the full question with all the hypotheses? 14:15

Q Sure. 14:15

Let's go back to Figure 1A of the '060 patent. 14:15

A Okay. 14:16

Q And you see that there are three array dies 110 here? 14:16
A Yes, I see that. 14:16
Q That share a common data die interconnect 120? 14:16
A I see that. 14:16
Q Okay. And the question is: If we have a scenario where two of the three dies are outputting data at the same time, does that cause potential for bus conflict? 14:16
MR. RUECKHEIM: Object to the form. 14:16
THE WITNESS: I believe a bus conflict is when they're outputting data in opposite -- opposite values. And I believe that if they both drive the bus at different values at the same time, there -- I would call that a bus conflict. 14:16
However, in certain designs, it is not unusual to have such conflicts occur for very short periods of time as you transfer control from one array die to another between reads or writes or whatever. And the potential damage of conflicts is ameliorated or eliminated by design. 14:17
So that's -- that's my answer. 14:17
MR. TEZYAN: Right. 14:17
Q But I think baked in your answer is -- is -- 14:17

person of ordinary skill in the art drive only one of the array die to avoid conflict with the other two array die, for instance? 14:18
A Your question -- 14:19
MR. RUECKHEIM: Objection to form. 14:19
THE WITNESS: -- started -- I'm sorry. 14:19
Your question started "in that circumstance." I need to know what you're talking about. That -- that's a little vague right now. 14:19
MR. TEZYAN: Okay. 14:19
Q Going back to Figure 1A, we see that there are three array dies in this stack; right? 14:19
A Yes. 14:19
Q And let's say you only wanted to derive from the top array die a signal. 14:19
A Okay. 14:19
Q And one way to do that to avoid interference and data collision would be to disable dies -- the middle die and the bottom die; right? 14:19
A Well, you would prevent them from driving. And you said disable. Whatever you did to prevent them from driving is what I would say you would do. 14:19
Q Okay. And to prevent them from driving, you could disable the data ports on the array dies; right? 14:20
A Yes, you could. 14:20

or let me put it this way -- sorry. Strike that. 14:17
What I'm asking is: Can array die 110 -- let's call the first one -- or I'm sorry. Strike that. 14:17
Can two of the array dies output data at the same time? 14:17
That's the question. 14:17
A Well, I just gave you an answer where they're both outputting data at the same time. I -- I don't know why that's not responsive. 14:17
Q In -- in part, I think your response said it's not unusual to have such conflicts occur for short periods of time as you transfer control away from one die to another. 14:18
So do you mean, by that, that there is some sort of delay time there? 14:18
A No. They could be both driving concurrently, but not for very long. And you design the chip to allow that -- I mean, the drivers and whatever, you -- you design them to allow this to occur. 14:18
Q Okay. But in general, you want to avoid having them drive concurrently; right? 14:18
A I think a person of ordinary skill in the art would try to avoid the driver collision. 14:18
Q Okay. So in that circumstance, would a 14:18

Q Okay. And for those two array dies that have their data ports disabled, are those still in electrical communication with the die interconnect? 14:20
MR. RUECKHEIM: Object to the form. 14:20
THE WITNESS: The data port -- yes. The data port is in electrical communication with the driver in this sense. It has a termination. 14:20
And the wave from the -- let's say the top die goes down the die interconnect. It reaches the second level, goes on the second level, goes toward the data port, hits it, and bounces around, back to the 110, up and down. And likewise, it continues down to the first level, goes out to the data port, bounces around, and comes down. 14:20
Now, at the data port, the data port isn't driving that line. But because the data port is connected to the -- to the trace on that array die, the wave will reach the driver and bounce back, and that driver has to be terminated in some way. Maybe it's infinite. Maybe it's got a resistor. But the wave will go back and will go from the die interconnect and go to the driver that's been disabled and bounce. 14:21
So if you ask, is the driver in the electrical communication? Absolutely, because the 14:21

wave is bouncing off the driver. 14:21
MR. TEZYAN: Okay. 14:21
Q And does that mean that the array dies, if 14:21
their data ports are disabled, are still in electrical 14:22
communication with the die interconnect? 14:22
MR. RUECKHEIM: Object to the form. 14:22
THE WITNESS: I think your question -- I'm 14:22
not sure what the question is. 14:22
MR. TEZYAN: Sure. 14:22
Q So your explanation was essentially that the 14:22
data port, despite being disabled, is in electrical 14:22
communication with the die interconnect; is that fair? 14:22
MR. RUECKHEIM: Object to the form. 14:22
THE WITNESS: I think that's -- that would be 14:22
fair. Go ahead. 14:22
MR. TEZYAN: Okay. 14:22
Q And then my follow-up question to that is: 14:22
Does that mean that the array dies with the data ports 14:22
that are disabled are still in electrical 14:22
communication with the die interconnect? 14:22
MR. RUECKHEIM: Object to the form. 14:22
THE WITNESS: There's a figure in this patent 14:22
that describes that. Let me -- let me show you the 14:22
figure. 14:22
Whoops. 14:23

What I was looking for is a figure in a 14:23
different patent. The -- there is on-die termination. 14:23
And the on-die termination is an electrical 14:23
communication and an electrical connection with the 14:23
die interconnect even when it's terminating a data 14:23
port that has been disabled. Okay. 14:23
So if -- if your question is, am I -- is any 14:23
part of the data port in electrical communication? 14:23
The answer is yes. 14:23
Is the ability of the driver to drive that 14:23
electrical communication when it's disabled? No. 14:24
So if -- I have to divide your question into 14:24
two parts. The driver as a whole, any -- any 14:24
component of electrical communication versus the 14:24
active driver in electrical communication. 14:24
And the answers could be different, depending 14:24
what you -- which part you're talking about. 14:24
MR. TEZYAN: Okay. 14:24
Q Let me ask a different question. 14:24
A Okay. 14:24
Q Going back to Figure 1A, you see the 14:24
driver 134 on the control die? 14:24
A Okay. 14:24
Q Will driver 134 still experience a load 14:24
that's attributable to the array die if the data port 14:24

for that array die is disabled? 14:24
A Yes. 14:24
MR. RUECKHEIM: Objection to form. 14:24
MR. TEZYAN: Q. And why is that? 14:24
A Well, there -- there are two aspects. 14:25
First of all, as taught by the patent, load 14:25
is capacitive. Okay. The line that goes from the 14:25
interconnect -- die interconnect 110 to the driver has 14:25
capacitance. You have to charge or discharge a 14:25
capacitance, regardless if the driver is active. 14:25
In other words, let the top layer have a 14:25
driver that sends a wave down the die interconnect. 14:25
Let the second layer be on a die interconnect in which 14:25
the driver is disabled. 14:25
That second layer still has capacitance 14:25
between the die interconnect and the driver on that 14:25
array die. And therefore, you have to charge or 14:25
discharge it. And therefore, it's in electrical 14:26
communication. 14:26
But even more, even more, the driver that's 14:26
drive -- that's about to drive the die 14:26
interconnect 110, let's say on the second or first or 14:26
the third layer -- layer, that driver is terminated. 14:26
It has a resistor. Sometimes it's called on-die 14:26
termination. That has a resistor. That could be 14:26

connected, and that connection could be -- receive the 14:26
wave that's coming from the die interconnect when the 14:26
wave is in electrical communication, and that as a 14:26
result, that on-die termination changes the reflection 14:26
that goes back. 14:26
If you terminate on die one way, you might 14:26
get no reflection. If you terminate another way, you 14:26
might get a re- -- a reflection. But that reflection 14:26
is an instance of communication. Okay. 14:27
So is it an electrical communication? You 14:27
bet. That's my answer. 14:27
Q Okay. Just to clarify, is the die 14:27
interconnect an electrical communication with the 14:27
array die when the data port for the die is disabled? 14:27
MR. RUECKHEIM: Object to the form. 14:27
THE WITNESS: I -- you -- you just repeated 14:27
the question. I -- I can repeat the answer. 14:27
But my answer was, yes, it is, because of the 14:27
wave that goes back and forth when you -- when you 14:27
initiate a transaction. 14:27
I'd like to bring up Exhibit 7 or 8, my book, 14:27
again. I'll show you that picture. 14:28
MR. TEZYAN: Okay. Okay. There was no -- 14:28
there was no question pending, sir. So we can -- we 14:28
can park that. And your counsel -- 14:28

THE WITNESS: Okay. 14:28
MR. TEZYAN: -- can ask you as many questions 14:28
as he wants about that on redirect. 14:28
Q But I'm about to ask another question, so if 14:28
you'd bear with me. 14:28
A Was there a question? 14:28
Q I'm about to ask another question. But if 14:28
you'll bear with me just a moment. 14:28
A I'm -- I'm not sure what you're asking me to 14:28
do or not do. What -- what is it? 14:28
MR. RUECKHEIM: I think he's saying there's 14:28
no -- no question pending. 14:28
THE WITNESS: No question pending. Okay. 14:28
MR. TEZYAN: Q. Can you please go to 14:28
paragraph 32 of your declaration. 14:28
A Okay. I'm at 32. 14:28
Q Okay. In the first sentence of paragraph 32, 14:29
you say: 14:29
"In the example of Fig. 2, 'die interconnect 14:29
220a" -- "'may be in electrical communication with a 14:29
data port from array die 210a.'" 14:29
Do you see that? 14:29
A I see that. 14:29
Q Okay. And then in the following sentence, 14:29
you say: 14:29

"Die interconnect" -- 14:30
I'm sorry. One moment. Okay. 14:30
So in -- sorry. Strike that. 14:30
Is there a difference between saying die 14:30
interconnect 220a is in electrical communication with 14:30
the data port from array die 210, versus die 14:30
interconnect 220a is in electrical communication with 14:30
array die 210? 14:31
A That's hard for me to parse out. Now that I 14:31
got the question, I know what to listen for and try to 14:31
figure out -- 14:31
Q Yeah, let me -- let me -- sorry. That was a 14:31
bad question. 14:31
So in paragraph 32, you say, quoting the 14:31
patent: 14:31
"'Die interconnect 220a" -- "'may be in 14:31
electrical communication with a data port from array 14:31
die 210a.'" 14:31
And what I want to know is: Do you think, as 14:31
a person of ordinary skill in the art, that there is a 14:31
difference between being in electrical communication 14:31
with a data port from array die versus being in 14:31
electrical communication with the array die? 14:31
A Yes. 14:31
Q And what's that difference? 14:31

A There's a difference. 14:31
Okay. Say -- what was the second question? 14:31
Q My follow-up question was: What is that 14:31
difference? 14:31
A Well, let's assume that there is a stub on 14:31
the -- on the array die that goes from the data 14:32
interconnect towards the data port. And when you make 14:32
an electrical connection for it to -- to sustain an 14:32
electrical communication, that stub is connected to 14:32
the driver. That stub will -- let's see -- that stub 14:32
will be in electrical communication with the data 14:32
port. 14:32
Now, suppose you don't connect the stub to 14:32
the data port. There's a gap between the stub and 14:32
the -- and the data port. In that case, it is not in 14:32
electrical communication with the data port, nor is 14:33
it, in fact, electrically connected to the data port. 14:33
So that's -- that's my distinction. 14:33
Q Okay. Let's go back to Figure 1A, if we can. 14:33
I just have a quick follow-up question on something 14:33
you said previously. 14:33
A Just a moment. Now -- got it. 14:33
Q So you testified that even if the array die 14:34
are disabled, it was disabled -- I'm sorry. Let me 14:34
repeat the question. 14:34

You testified earlier that if the data ports 14:34
for an array die are disabled, there is still a load 14:34
that's exerted on driver 134; right? 14:34
A That's correct. 14:34
Q Okay. Is the load reduced from a scenario 14:34
where those drivers would be enabled? 14:34
A Load reduced? 14:34
Because of on-die termination and because 14:35
the -- the on-die termination can change in time, it's 14:35
controlled, I -- I don't know whether the load will be 14:35
higher or greater or the same. It -- it's up in the 14:35
air, so to speak. I don't have enough information to 14:35
answer that question. 14:35
Q What would it depend on? 14:35
A Well, the load of the driver, when it's -- 14:35
when it potentially can drive this -- this 110 depends 14:35
on this -- on the termination at the driver. And the 14:35
load that an external driver sees when the wave goes 14:35
down to -- down the die interconnect to reach that 14:35
driver depends on the load that the driver presents. 14:35
That load depends on the on-die termination. So I 14:35
can't tell what that is. 14:36
Q Does the on-die termination load change if 14:36
the driver is disabled or enabled? 14:36
A That depends. I -- I don't know the answer. 14:36

Q Could you pull up Figure 2B from the '060 patent. 14:36
A 2B? 14:36
Q I'm sorry. Figure 2. There is no Figure 2B. 14:36
A Of this patent? 14:37
Q Yes, sir. 14:37
A I have Figure 2. Okay. I've got Figure 2. 14:37
Q Okay. And 210a through d, these are the array dies; correct? 14:37
A Yes. 14:37
Let me do something. Okay. I see it all now. Okay. 14:37
Q And 220a, that's a die interconnect; right? 14:37
A 220a is a die interconnect. That's correct. 14:37
Q And these black circles through the array dies, that represents where the die interconnect is in electrical communication with the array die; is that correct? 14:37
A That's correct. That's correct. 14:37
Q Okay. So in Figure 2, array dies 210a and 220b are in electrical communication with die interconnect 220a; right? 14:37
A That's correct. 14:38
Q And earlier, we were discussing the concept of rank. 14:38

Do you remember that discussion? 14:38
A I do. 14:38
Q Now, could array dies 210a and 210b belong to the same rank? 14:38
MR. RUECKHEIM: Object to the form. 14:38
THE WITNESS: I don't have enough information to answer that question. 14:38
MR. TEZYAN: Q. What additional information would you need? 14:38
A I don't see the layout of ranks on those array dies. 14:38
Q Is there any reason it could not belong to the same rank? 14:38
A Let me hypothesize. If there are two ranks laid out on these two die interconnects, one rank is totally on one die -- array die, and the other rank is totally on the other array die. Okay. So they would -- what's on one die would not belong to the rank that's on another die. 14:38
That's -- that's just one possibility. But there are other ways you can lay it out. 14:39
Q Right. 14:39
And is one of those other ways that array dies 210a and 210b could belong to the same rank? 14:39
MR. RUECKHEIM: Object to the form. 14:39

THE WITNESS: If the system is set up so that a logical rank is broken in two pieces, one piece on one die inter- -- one array die, one piece on another array die; then if you accessed that rank sequentially by picking off the half that's in the lower die, subsequently picking off the part that's in the upper die, then you could do that. That -- that's an easy way. 14:39
MR. TEZYAN: Q. You used the term "logical rank" there. What does that mean? 14:40
A The rank appears to the memory controller on the other end of the system bus as being one cohesive rank. The controller doesn't know that actually, that rank is split on two different layers of a mem- -- of a memory. 14:40
So when it asks to read a rank, the rank is delivered in one piece to the memory controller, but is ac- -- actually accessed in two pieces at the memory cells. 14:40
Q Okay. But could array dies 210a and 210b be part of the same physical rank? 14:40
MR. RUECKHEIM: Object to the form. 14:40
MR. TEZYAN: Let me back up. Let me withdraw the question. 14:40
Q What does a physical rank mean? 14:41

MR. RUECKHEIM: Object to the form. 14:41
THE WITNESS: Physical rank has changed over time. So I think one of ordinary skill in the art would believe a physical rank to be a layout of the cells physically. That's -- that's the best I can answer that. 14:41
MR. TEZYAN: Okay. 14:41
Q And with that understanding of physical rank, could 210a and 210b belong to the same physical rank? 14:41
MR. RUECKHEIM: Same objection. 14:41
THE WITNESS: I said that the notion of physical rank has changed over time. And one could decide to design a memory in which physical rank is split between two -- two layers of a memory cell. And that by doing it, your physical rank that's split between these two layers can imitate a physical rank memory cell, a memory cell where the physical rank is on one layer. 14:41
And I think that would be reasonable for a person of ordinary skill in the art to understand at the time of the patent. 14:42
MR. TEZYAN: Okay. 14:42
Q So assuming array die 210a and 210b are in the same physical rank, how would they output data in parallel in response to a read command if they share 14:42

only one die interconnect? 14:42
MR. RUECKHEIM: Object to the form. 14:42
THE WITNESS: In this case, you show one die 14:42
interconnect connecting those two -- those two layers. 14:43
In fact, you could have a die interconnect for all the 14:43
bits in a word. I mean, one -- each bit having its 14:43
own individual die interconnect connecting those two 14:43
layers, in which case the lowest layer could be 14:43
outputting data on one set of die interconnects, while 14:43
the layer above it outputs data on the other set of 14:43
die interconnects at the same time. 14:43
MR. TEZYAN: Okay. 14:43
Q But in the configuration we have here where 14:43
there is one die interconnect for data between 210a 14:43
and 210b, and assuming that 210a and 210b are in the 14:43
same physical rank, would it be possible to output 14:43
data in parallel in response to a read command? 14:44
A Yeah, you -- if they're the same physical 14:44
rank. That doesn't mean they'll be driving the same 14:44
die interconnect. Just put them on different die 14:44
interconnects. 14:44
Q In this configuration, though, they share the 14:44
same die interconnect; right? 14:44
A Yeah, but you're making an assumption that 14:44
it's -- it becomes unreasonable. You can -- you can 14:44

make an assumption for something that you can't build. 14:44
Okay. 14:44
And if you're telling me that you have a 14:44
physical data on two die layers -- two array die 14:44
layers, and they're all going to drive the same die 14:44
interconnect at the same time, you know, I could say, 14:44
Hey, yeah, that looks very strange. I don't think you 14:44
can build that. 14:45
So your hypothesis is bothering me. It's not 14:45
something that I would encounter. A person of 14:45
ordinary skill in the art would say, What are you 14:45
doing here? 14:45
So that's -- that's my answer. 14:45
Q Okay. I'm trying to understand why that's 14:45
your answer. 14:45
So is it what we talked about earlier, that 14:45
the risk of data collision in such a scenario prevents 14:45
you from sort of sharing a common die interconnect for 14:45
the 210a and 210b that are in the same physical rank 14:45
there? 14:45
MR. RUECKHEIM: Object to the form. 14:45
THE WITNESS: I testified that it's -- it is 14:45
the issue of collision that -- that bothers me. 14:45
And I also testified that they can -- the two 14:45
bits that are driving the same line at the same time 14:45

could happen when there -- when one is ending its 14:45
burst of data and the other one is beginning. That 14:45
actually happens in memory chips so that momentarily, 14:46
the drivers on those two layers, both belonging to the 14:46
same rank, can be driving at the same time. You just 14:46
have to be careful with the timing and the way the 14:46
load is set up. You can design for that. 14:46
(Document remotely marked Exhibit 11 14:47
for identification.) 14:47
MR. TEZYAN: I've introduced Exhibit 11. 14:47
Q Can you please refresh your Exhibit Share. 14:47
A Okay. 14:47
Q And let me know when you have it. 14:47
A Okay. I have refreshed. I see that I can 14:48
access Exhibit 11. I'm about to download. 14:48
Okay. I have Exhibit 11 in my reader. 14:48
Q Okay. And Exhibit 11 is U.S. Patent 14:49
Application No. 2011/0103156 to Kim et al.; right? 14:49
A That's correct. 14:49
Q And according to the Abstract, Kim discloses: 14:49
"A data input/output circuit includes a rank 14:49
selecting section and a data input/output section." 14:49
Right? 14:49
A I haven't read this patent before. I have to 14:49
read it. 14:49

Q Okay. Take your time. But I'm just asking 14:49
you to confirm what the Abstract says. 14:49
A So you're only going to ask me about the 14:49
Abstract; is that it? 14:49
Q For now, yes. 14:49
A Okay. 14:49
Q But if you'd like to take a minute and review 14:49
it, you can go ahead. 14:49
A I would like to. 14:49
Q Please. 14:49
A Okay. I -- I think I understand some aspects 14:51
of it. I might not be able to answer your question, 14:51
but go ahead. 14:51
Q I'll just repeat what my first question was: 14:51
According to the Abstract, Kim discloses: 14:51
"A data input/output circuit includes a rank 14:51
selecting section and a data input/output section." 14:51
Right? 14:51
A That is correct. 14:51
Q Okay. And: 14:51
"The rank selecting section is selectively 14:51
connected to one of the first and second ranks in 14:51
response to a chip selection signal, and outputs data 14:52
to a connected rank or receives data from the 14:52
connected rank." 14:52

Did I read that correctly? 14:52
A You did. 14:52
Q Okay. So the use of chip select signals for 14:52
rank selection is common in DRAM-based memory systems; 14:52
right? 14:52
A It -- it's -- yes, it's -- it's -- it's used 14:52
in practice. 14:52
Q Okay. So fair to say that Kim is discussing 14:52
a DRAM-based memory system? 14:52
MR. RUECKHEIM: Object to the form; beyond 14:52
the scope. 14:52
THE WITNESS: Okay. Would you repeat your 14:52
question, please. 14:53
MR. TEZYAN: Sure. 14:53
Q The question was: Is it fair to say that Kim 14:53
is discussing a DRAM-based memory system -- 14:53
A I just searched. I did not see any reference 14:53
to D-R-A-M, DRAM. So I'd have to read the patent 14:53
carefully to decide if it's talking about DRAM or 14:54
something else. 14:54
Q Okay. Designs for DRAM memory system 14:54
organization, can they readily be applied to other 14:54
types of memory systems, such as SRAM or NAND? 14:54
Let me -- let me withdraw the question. 14:54
Sorry. So let me ask it slightly differently. 14:54

So there are other types of -- sorry. 14:54
There are multiple types of memory systems, 14:54
right, such as SRAM? 14:54
A That's correct. 14:54
Q And NAND is another type of memory system? 14:54
A That's correct. 14:54
Q N-O-R, is that another type of memory system? 14:54
A Can you -- for the record, can you just tell 14:55
me what the acronym is? 14:55
Q NOR is another type of non-volatile -- 14:55
A Yes, because it's NAND and NOR, yes. 14:55
Q Yes. Okay. 14:55
So designs for DRAM memory systems can be 14:55
readily applied to these other non-DRAM memory 14:55
systems: SRAM, NAND, NOR; right? 14:55
A No. No. 14:55
I'm sorry. Did you hear me? I said, "No." 14:56
Q Oh, yes, I heard you. Sorry. I'm just 14:56
gathering my thoughts. 14:56
Why don't we go ahead and take a quick break. 14:56
A Okay. 14:56
THE VIDEOGRAPHER: We are going off the 14:56
record. The time is 2:56 p.m. 14:56
And this is the end of Media Unit No. 6. 14:56
(Recess taken.) 14:56

THE VIDEOGRAPHER: We are going back on the 15:06
record. The time is 3:06 p.m. 15:06
And this is the start of Media Unit No. 7. 15:06
(Document remotely marked Exhibit 12 15:06
for identification.) 15:06
MR. TEZYAN: I'm going to go ahead and upload 15:06
a new exhibit. 15:06
Q Dr. Stone, could you please refresh your 15:06
Exhibit Share, and let me know when it comes up, 15:06
please. 15:07
A Okay. I see Exhibit 11. I'm about to 15:07
download. 15:07
Q It should be Exhibit 12, I believe. 15:07
A All right. 15:07
We actually already had that one. All right. 15:07
Try it again. 15:07
Ah, I've got 12. I am about to download. 15:07
Q Let me know when you have it, please. 15:08
A I am just -- I have it now. I have it in 15:08
front of me. 15:08
Q Okay. And this is U.S. Patent Application 15:08
2011/0026293 to Riho; is that correct? 15:08
A That's correct. That's what I see. 15:08
Q Okay. And I'd just like to bring up an 15:08
example just to get a -- make sure I understand your 15:08

testimony with electrical communication and not an 15:08
electrical communication. 15:08
A Okay. 15:08
Q If you'll just bear with me for a few 15:08
minutes. 15:08
So if you'd go to paragraph 69. 15:08
And by the way, I'm -- why don't you take a 15:08
minute or two and just read this before I launch into 15:08
the description. 15:08
A I'd like to. 15:08
When you said "69," would that be in my 15:08
report? 15:08
Q Yes, I'm -- what's that? 15:08
Oh, no. Paragraph 69 of -- of this exhibit, 15:09
sir. 15:09
A There's paragraph 69. Okay. Let me look. 15:09
(Reading document.) 15:12
Okay. I'm ready. 15:12
Q Okay. So referring to Figure 4 of Riho. 15:12
A Okay. 15:12
Q Can we agree, based on the description, that 15:12
only SDRAM device D15 and D7 are on? 15:13
A Well, point me to the description. I -- I 15:13
looked at the patent, but I'm not -- I can't -- I 15:13
can't comment until you tell me what to look at. 15:13

Q Fair enough. 15:13
So for starters, in Figure 4 for the 15:13
SDRAM D15 that's connected to TSV15, you see that it 15:13
says "ON"; correct? 15:13
A Okay. 15:13
Q And then go ahead and review paragraph 74. 15:13
A There's a lot here. I mean, it -- in 74, 15:14
there's a context that I haven't read. It's -- this 15:14
is going to be very difficult for me to comment on in 15:14
such a short time. 15:14
Q Okay. Well, let's go to paragraph 72, okay, 15:14
where the switch -- the set indication signal for the 15:15
chip switch circuit is described. And I'm talking 15:15
about D715. 15:15
A I see D715, yes. 15:15
Q Okay. And in the next paragraph, in 73, it 15:15
says that: 15:15
"In the chip switch circuit CS7 of the 15:15
SDRAM D7" -- and -- "SDRAM D15, the switch sa which is 15:15
given the set indication signal D715 and the second 15:15
group" -- "is put in an off state." 15:15
Right? 15:15
A The conversely bothers me. There's something 15:15
I haven't read about the opposite of that. Is it in 15:15
72? 15:15

"The memory system 1010." 15:18
Is that correct? 15:18
Q Yeah, that's correct. 15:18
Could you review this passage to yourself. 15:18
A Yes, I will. 15:18
(Reading document.) 15:18
And the passage you referred to is just that 15:19
one paragraph; is that correct? 15:19
Q Yes, sir. The paragraph that ends on 15:19
column 25, line 7. 15:19
A That's fine. I have reviewed it. 15:19
Q Okay. So the passage says that: 15:19
"The memory system 1010 may transition from 15:19
the first state to the second state in response to a 15:19
trigger condition, such as when the memory system 1010 15:19
detects that there is a power interruption (e.g., 15:19
power failure or reduction) or a system hang-up." 15:19
Right? 15:19
A That's correct. 15:19
Q So would a person of ordinary skill in the 15:19
art understand that in the second state, the module 15:19
may be in, for example, a power failure? 15:19
MR. RUECKHEIM: Object to the form. 15:19
THE WITNESS: Ask your question again, 15:20
please. 15:20

Q Uh-huh. 15:15
A (Reading document.) 15:15
Okay. I vaguely understand what's going on, 15:16
but go ahead. 15:16
Q Okay. So returning to Figure 4, so do you 15:16
understand from that description that SDRAM 15 along 15:16
TSV15 is enabled? 15:16
MR. RUECKHEIM: Object to the form, and 15:16
beyond the scope. 15:16
THE WITNESS: I'm sorry. All I saw in the 15:16
description was something was turned on. Something 15:16
was turned off. I -- I -- I don't see the 15:16
connectivity yet. 15:16
I need to look at this patent and study it. 15:16
I -- I'm sorry. I -- very difficult for me to answer 15:17
these questions. 15:17
MR. TEZYAN: Q. Can you please return to the 15:17
'918 patent. 15:17
A Exhibit what? 15:17
Q That is Exhibit 4. 15:17
A I have it. 15:17
Q Okay. And if you'll bear with me just a 15:17
second. 15:17
Could you please go to column 24, line 60. 15:18
A Okay. I see at line 60. It starts: 15:18

MR. TEZYAN: Q. Would a person of ordinary 15:20
skill in the art understand that in the second state, 15:20
the memory module may be in, for example, a power 15:20
failure? 15:20
MR. RUECKHEIM: Same objection. 15:20
THE WITNESS: I'm reading the text, and it 15:20
says that it may transition from the first state to 15:20
the second state, such as when the memory system 15:20
detects that there is a power interruption; for 15:20
example, power failure. 15:20
I think that what you're asking is, is it 15:20
true that the patent teaches that? 15:20
As far as I can tell, the answer is yes. 15:20
MR. TEZYAN: Okay. Let me ask a slightly 15:20
different question then. 15:21
Q Does the patent teach that the memory module 15:21
in the second operable state can be a state in which 15:21
there is a power reduction? 15:21
MR. RUECKHEIM: Object to the form, and 15:21
beyond the scope. 15:21
THE WITNESS: A power reduction? 15:21
(Reading document.) 15:21
I'm looking at information that may be useful 15:21
to answer at column 20. And the information says the 15:22
trigger condition -- it describes a trigger condition 15:23

in the first sentence, and it says that the -- for example, power failure. 15:23

So I'm informed that the trigger condition can be a power failure. It does describe certain embodiments, but it doesn't describe for all. 15:23

Then it says something about the power module may switch, but it doesn't relate the switch to the trigger condition. It says that the -- when no power failure is detected, the power module may provide power to certain components, maybe not others. 15:23

So it -- the power module trigger could be a power failure, but it's not necessarily, and it may not be in every embodiment. So I -- I don't have a firm view of what the trigger condition might be. 15:23

MR. TEZYAN: I'll just object that that's nonresponsive, because I didn't ask about the trigger condition, and I'll move to strike. 15:24

THE WITNESS: Well, I'm sorry. Ask your question again, and I'll do it my best to answer it. 15:24

MR. TEZYAN: Yeah. No problem. 15:24

Q Let me direct your attention back to column 24. And actually, more specifically, column 25. This is line 3 through 7. 15:24

And -- and so one example here that it discusses with the trigger condition is a power 15:24

reduction; right? 15:24

It says: 15:24

"(e.g., power failure or reduction)." 15:24

A That's -- 15:24

Q Correct? 15:24

A -- that's correct. That's right. 15:24

Q Okay. So with that in mind, does the patent teach that the memory module in the second operable state can be a state in which there is a power reduction? 15:24

MR. RUECKHEIM: Object to the form. 15:24

THE WITNESS: Ask your question again, please. 15:25

MR. TEZYAN: Sure. 15:25

Q Does the patent teach that the memory module in the second operable state could be in a state where there is a power reduction? 15:25

MR. RUECKHEIM: Object to the form. 15:25

THE WITNESS: Are you talking about the whole memory module? 15:25

MR. TEZYAN: Correct, sir. 15:25

THE WITNESS: And your question again was, if you have a power interruption, something happens. What was the hypothesis? 15:26

If you have a power reduction, then -- 15:26

MR. TEZYAN: Q. So the question was: Does the patent teach that the memory module in the second operable state could be in a state where there's a power reduction? 15:26

MR. RUECKHEIM: Object to the form. 15:26

THE WITNESS: I'm informed by lines 54 through 58 of that same paragraph -- of the same column 25 -- let me see. 15:26

Oh, I'm sorry. I messed it up. 15:28

At line 54, it says: 15:28

"Power may be supplied to the volatile memory subsystem 1030 from a first power supply (e.g., a system power supply) when the memory system 1010 is in the first state and from a second power supply 1080 when the memory system 1010 is in the second state." 15:28

So this question is when the power supply is in the second state, it can supply power to the volatile memory system. And from what we saw earlier, it can reach that second state by a power reduction. And that's -- I think that teaches what you're asking about. 15:29

MR. TEZYAN: Yeah, let me just -- my -- my question is not intended to be tricky, sir. So let me just make it a little clearer. 15:29

Q If we'd go back to row 3 -- sorry -- line 3 15:29

of column 25, right, it says that: 15:29

"The memory system 1010 may transition from the first state to the second state in response to a trigger condition, such as when the memory system 1010 detects that there is a power interruption (e.g., power failure or reduction) or a system hang-up." 15:29

And my question is: Would a person of ordinary skill in the art reading the specification of the '918 patent understand that the second operable state could refer to a state in which there is a power reduction? 15:29

MR. RUECKHEIM: Object to the form. 15:30

THE WITNESS: There are lots of "if"s and "but"s and things. It may transition, and this is in certain embodiments. All I can say is that in certain embodiments, there may be a transition to the second state when there is a power reduction. 15:30

MR. TEZYAN: Q. Memory modules typically have memory devices on them; right? 15:30

A Yes, that is correct. 15:31

Q And -- and those memory devices require power to operate; right? 15:31

A No. 15:31

Q They can operate without power? 15:31

A Well, your word "operate" bothers me. 15:31

There's non-volatile memory, and part of its operation is storage. It's true that non-volatile memory can store data without power. 15:31

Q Okay. So let's just say on a memory module, we have volatile memory and non-volatile memory; right? 15:31

A You'll have to repeat that. 15:31

Q Let's say on a memory module, we have volatile memory and non-volatile memory? 15:32

A It has volatile and non-volatile memory on this module? 15:32

Q Yes. 15:32

A Yes. 15:32

Q The volatile memory will require power to operate; is that right? 15:32

A Yes. 15:32

Q Okay. So if there is a power loss, the volatile memory will no longer operate; is that right? 15:32

A The answer is "yes" and "no." 15:32

Q What do you mean? 15:32

A When you say "will no longer operate," the answer is, it will be able to operate for a little bit, for a while. Okay. 15:32

Q Why would it be able to operate for a while? 15:32

A When there is a power failure, there may be 15:32

enough voltage available in storage devices sitting around that will supply the power needed to operate it until those storage devices and capacitors and whatever exhaust their reserve power. 15:32 15:33 15:33 15:33

Q Okay. So in that scenario, the memory -- sorry. Let me make that question clearer. I withdraw. 15:33 15:33 15:33

So in that scenario, the volatile memory would still be operating; right? 15:33 15:33

A Which scenario, now? 15:33

Q The scenario where there is a power failure, it's your testimony that the volatile memory would still be operating; right? 15:33 15:33 15:33

A For a while, not -- not indefinitely. 15:33

Q And the non-volatile memory would be operating as well; right? 15:33 15:33

A In the sense that its operation allows it to store data without losing it. And in that -- if that satisfies your definition of operation, it will be operating. 15:34 15:34 15:34 15:34

Q What are some examples of non-volatile memory? 15:34 15:34

A Flash memory. 15:34

Q Is a register an example of non-volatile memory? 15:34 15:34

A Depends. 15:34

Q Depends on what? 15:34

A The register can be maintained in a state after you lose power if it is programmed to -- like in an FPGA, to retain state when it loses power. And you can do that essentially by storing or not storing charge in various places. 15:34 15:34 15:34 15:34 15:34

Q Okay. So would a person of ordinary skill in the art understand that a non-volatile memory that's part of an FPGA could be a register? 15:34 15:35 15:35

MR. RUECKHEIM: Object to the form. 15:35

THE WITNESS: I think a person of ordinary skill in the art, if asked that question, would consider the options of how one might build that and would decide, Yeah, I can build a register that is non-volatile on an FPGA if I could do this and this and this on the FPGA. 15:35 15:35 15:35 15:35 15:35

MR. TEZYAN: Q. Let's jump to paragraph 37 of your declaration. And that's Exhibit 1. 15:35 15:36

A I'm at 37, and this is the proposed construction for driver size. 15:36 15:36

Q Yes, sir. 15:36

So Micron's proposed construction is that: 15:36

"The physical dimensions of the second driver being different from the physical dimensions of the 15:36 15:36

first driver." 15:36

Do I have that right? 15:36

A You do. 15:36

Q What do you mean by "physical dimensions"? 15:36

A Physical dimension is length, width, area, the physical size of the driver on the die. 15:36 15:37

Q What is it that you believe the physical size is comprised of? 15:37 15:37

MR. RUECKHEIM: Object to the form. 15:37

THE WITNESS: You measure it. You -- you look at the driver on the die, and you find it's so many millimeters by so many millimeters. Those are physical dimensions. 15:37 15:37 15:37 15:37

MR. TEZYAN: Okay. 15:37

Q Let's jump to paragraph 42 of your declaration. 15:38 15:38

A Okay. Okay. 15:38

Q And you say that: 15:38

"'Driver size' refers to the physical dimensions of the driver such as the following portions of the specification below which refers to the amount of space a driver takes up on a die or the number of physical transistors directly relating to the size of the die." 15:38 15:38 15:38 15:38 15:38 15:38

Is that right? 15:38

A That's what I say. That's correct. 15:38
Q Okay. So if you have a driver circuit that 15:38
has a set of transistors, what is the size of that 15:38
driver circuit? 15:38
A It's the physical dimension of the driver. 15:39
Q So is it the combination of those two 15:39
transistors? 15:39
A Those two transistors will lie in an area 15:39
that you identify as the driver. The size of the 15:39
driver is the -- is related to the length and width of 15:39
that area that -- that encloses those transistors. 15:39
Q Okay. Let me put it another way. Say you 15:39
have a driver circuit that comprises a number of 15:39
transistors; let's say ten transistors. 15:39
A Okay. 15:39
Q And then for a particular load, you use a 15:39
subset of transistors; say, two transistors. And for 15:39
other loads, you use all of the transistors; i.e., ten 15:39
transistors. 15:40
Are you with me so far? 15:40
A So far. 15:40
Q Okay. In that circumstance, what is the 15:40
physical dimension of the driver? 15:40
A The length and width of the area that's 15:40
occupied by those transistors. 15:40

Q So all ten transistors? 15:40
A If they -- if they are in that driver, then 15:40
all ten transistors. 15:40
Q So are you saying that the driver size 15:40
doesn't depend on how many transistors are used to 15:40
actively drive a load? 15:40
A I think that's answered right here by the 15:40
patent itself. We're on the page. Okay. I would 15:40
like you to look at the top of page 15 in my report 15:40
where there's a quote. And it's the last sentence of 15:40
that quote says: 15:40
"However, generally a larger driver not only 15:40
consumes more space on the control die, but also 15:40
consumes more power." 15:41
Now, what this teaches is that we're talking 15:41
about space on the control die. And more often than 15:41
not, maybe when you have bigger space, you can do more 15:41
power. But it is distinguishing space from power or 15:41
strength. 15:41
We're not done. Go down. There are three 15:41
quotes on that page. Let's take a look at the last 15:41
quote. You see where they have bold text? Then after 15:41
the bold text, it says: 15:41
"A larger driver often consumes more power 15:41
than a smaller driver." 15:41

So again, it says that space and power that 15:41
you have are related, but they're not the same, and it 15:41
distinguishes the space from power. 15:41
But we're not even done yet. Let's open the 15:42
patent, the '160 patent. 15:42
Do we have an exhibit for it? 15:42
Or the '060. We have an '060, Exhibit 9. 15:42
Can we look there? 15:42
Q Sure. 15:42
A Just a moment. I'll still looking. 15:43
Q That's fine. Take your time. 15:43
A I got it. It's on -- it's on column 4. 15:43
Q Okay. 15:43
A Okay. Let me -- I lost it for a second. I 15:43
took my... 15:43
Ah, it's in column 17. I was looking in the 15:43
wrong place. 15:44
Q Okay. 15:44
A Oh, I think we already have this. 15:44
There was one other place. This is in my 15:44
report, column 17. 15:44
Q Uh-huh. 15:44
A A larger driver also consumes -- let me see 15:44
if I can find what I'm looking for. Now I know what 15:44
to look for. 15:45

Ah, I did find it. This is in column 4. I 15:45
just didn't see it. I'm looking at line 22: 15:45
"In certain embodiments, reducing one or both 15:45
of driver size and driver power consumption may be 15:45
accomplished by increasing the number of die 15:45
interconnects" -- 15:45
Et cetera, et cetera. 15:45
But I want to point out that this sentence 15:45
distinguishes driver size from driver power. They are 15:45
different. It says "one or both of." 15:46
So I've given you three places where the 15:46
patent teaches that size is what they're interested 15:46
in. And that's distinguished from power, but they're 15:46
related. That's my testimony. 15:46
Q Is driver power consumption the same thing as 15:46
driver strength? 15:46
A I haven't opined on that. Here, the patent 15:46
teaches about power. I think one of ordinary skill in 15:47
the art might believe that strength and power are 15:47
related. That's a reasonable position to take for a 15:47
person of ordinary skill in the art. If we get down 15:47
to places where they actually may be different, well, 15:47
okay. That can happen, too. 15:47
Q Okay. So just so the record is clear, 15:47
because I asked the short question and got a helpful 15:47

but long answer, is it your testimony that the driver size doesn't depend on how many transistors are actively being used? 15:47 15:48 15:48

A The driver size in this patent is taught to be the area of the driver or the physical dimensions of the driver. And so it does not depend on the number of transistors that are actually being used. 15:48 15:48 15:48 15:48

Q Okay. So if only two of the ten transistors are used to drive a load, is the physical size of the driver determined by the ten transistors or the two transistors? 15:48 15:48 15:48 15:48 15:48

A Are you saying that you'll never use transistors? Is that your assumption? 15:48 15:48

Q No. 15:48

I'm just saying for purposes of my hypothetical, right, you have a driver that's composed of ten transistors; right? 15:48 15:48 15:48

A I understand. 15:48

Q Okay. And for the particular load that's on this driver, you're using two of the ten transistors for driving. 15:48 15:49 15:49

Does that make sense? 15:49

A That makes sense. 15:49

Q Okay. So if only two of the ten transistors are used to drive a load, is the physical size of the 15:49 15:49 15:49

driver determined by the ten transistors or the two transistors? 15:49 15:49

A I asked a question: Do you ever turn on all ten transistors? 15:49 15:49

Q You could. But in this situation, you're just using two. 15:49 15:49

A I think you answered my question. If you can turn on all ten, the driver size is related to the load that you can drive. And if you're going to drive ten transistors, you have to have enough area to dissipate the power they generate. And once you have that area, even if you only use two, you've got the area, because you're committed to the area for the ten. 15:49 15:49 15:49 15:49 15:49 15:49 15:49 15:49 15:49 15:49

Q Okay. So the answer to my question is that if you have a driver that's composed of ten transistors, regardless of whether you're driving two or ten of them, the driver size is ten transistors? 15:49 15:49 15:49 15:50 15:50

A No. The driver size is the physical dimension of the driver. 15:50 15:50

Q Okay. Sorry. I withdraw the question. 15:50

So let me just ask the original question again: If only two of the ten transistors are used to drive a load, is the physical size of the driver determined by the ten transistors? 15:50 15:50 15:50 15:50

A I don't know exactly, but the answer is it could be. 15:50 15:50

Q Okay. When would it not be determined by those ten transistors? 15:50 15:50

A Ask your question again, because I think I misunderstood it. 15:50 15:50

Q Sure. 15:50

The -- the question is -- and I think I know the answer, based on your testimony, but I just want to make sure we're absolutely clear. 15:50 15:50 15:50

So if only two of the ten transistors are used to drive a load, is the physical size of the drive -- the driver determined by ten transistors or two transistors? 15:50 15:50 15:51 15:51

A My answer is going to be determined by the two transistors, because the size of the driver has to be able to dissipate the power of whatever is in there. And if those two transistors are driving like mad, and that would -- might be the case, then you have to make enough area to dissipate the heat. 15:51 15:51 15:51 15:51 15:51 15:51

You just told me that you're never going to drive the other eight, if I understand the hypothesis. 15:51 15:51

Q No. 15:51

So -- 15:51

A Okay. 15:51

Q -- I'll -- I'll -- I'll ask the question again: You have -- you have a driver that is comprised of ten transistors; right? 15:51 15:51 15:51

A Yes. 15:51

Q Okay. And you can use the ten transistors to drive a load, or you can use a subset of those transistors, in this example two, to drive a load. 15:51 15:51 15:51

A I understand. 15:52

Q Okay. In this hypothetical, is the physical size of the driver determined by the ten transistors or the two transistors? 15:52 15:52 15:52

A If you ever turn on the ten transistors, that's a heavier load than the two. You must design the driver to have an area that can dissipate the power of ten transistors all being on. 15:52 15:52 15:52 15:52

Q Okay. So regardless of whether it's the two transistors driving a load or the ten transistors driving a load, to you, it's just a single driver? 15:52 15:52 15:52

MR. RUECKHEIM: Object to the form. 15:52

THE WITNESS: I'm sorry. The -- I need to know the hypothesis. We have one -- one transistor in a driver; is that correct? 15:52 15:52 15:53

MR. TEZYAN: No. 15:53

Q So the -- it's -- it's the same example as before where you have a ten-transistor driver, right, 15:53 15:53

where a subset of them can be used to drive the load, 15:53
or all ten can be used to drive the load; right? 15:53
A I got it. 15:53
Q Okay. And in -- in that example, you're 15:53
saying that it's the same driver of the same physical 15:53
size, whether you use the subset or whether you use 15:53
all ten of them; right? 15:53
A That's correct. 15:53
(Document remotely marked Exhibit 13 15:54
for identification.) 15:54
MR. TEZYAN: Q. Can you please refresh your 15:54
Exhibit Share. 15:54
A Okay. 15:54
Q I've marked another exhibit. It's 15:54
Exhibit 13. Please let me know when you have it. 15:54
A Okay. I see it in my -- in my computer as 15:54
the name of the document. I've just loaded it up, and 15:55
I'm about to download. 15:55
Okay. I've downloaded it. I'm about to open 15:55
it. 15:55
I have it open. 15:55
Q Okay. And this is U.S. Patent No. 7,969,192 15:55
to Wyman et al.; is that right? 15:55
A That's correct. 15:55
Q And I -- I mean, take -- take a minute to 15:55

look over the document. But I -- I just want to ask 15:55
you questions about the driver circuit that's depicted 15:55
in Figure 3, just to understand your testimony on 15:55
driver size. 15:55
A (Reading document.) 15:55
I have not studied this patent. This is 15:56
going to be hard to respond. I'll try. Go ahead and 15:56
ask your question. 15:57
Q Okay. My question has to do with Figure 3 of 15:57
Wyman. And in Figure 3, do you see the two triangles 15:57
in the center, 302-1 and 302-2? 15:57
A I do. 15:57
Q And those depict tristate driver circuits; 15:57
right? 15:57
And if you need to confirm that, you can go 15:57
to column 3, line 50. 15:57
A I see -- I see the enable 0 and enable 1 15:57
may -- so -- and the symbol is of a tristate driver. 15:57
Yes, I see that. 15:57
Q Okay. So if only 302-1 is enabled, what is 15:57
the size of the driver circuit? 15:57
MR. RUECKHEIM: Object to the form. 15:57
THE WITNESS: Okay. This is on the die, and 15:57
it's through manufacturing; is that correct? 15:58
MR. TEZYAN: Q. Why would that make a 15:58

difference? 15:58
A Well, if we're looking at a die that has a 15:58
certain physical area for the driver, I can answer 15:58
your question. But I don't know the context. I don't 15:58
understand your question. If the area is saying if 15:58
you enable 0 or if you enable both, I can't really 15:58
tell what you're talking about. 15:58
Q You're saying the area could vary if you 15:58
enabled one of the drivers versus enabling both of the 15:58
drivers? 15:58
A I'm asking you. Are you telling me the area 15:58
doesn't vary? Is that correct? 15:58
Q I'm -- I'm just asking you, sir, as a person 15:58
of ordinary skill in the art -- 15:58
A I haven't read the patent for sure. I don't 15:58
know if he's talking about being able to vary the area 15:59
at some point. 15:59
The selection could be at design time or it 15:59
could be in the field. If you're going to vary the 15:59
area at design time, then you would have drivers that 15:59
physically have different area on these -- on these 15:59
chips. But if -- if you fix the area at some point 15:59
and you vary the enables in the field, that's a 15:59
different story. 15:59
I don't know which one applies. 15:59

Q Are you saying you vary the size of the 15:59
enables in the field? Is that what you're saying? 15:59
A If there were a way to vary the size of that 15:59
device in the field in some fashion -- I don't know 15:59
how they would do it. I'm asking you, is that the 15:59
case? At design time, I would understand. But 15:59
maybe -- I haven't read the patent, so I don't know 15:59
about the area. You'll have -- I'm asking you what 16:00
the -- what the answer is to that question. 16:00
Q Okay. But how would the size of one of those 16:00
drivers be varied in the field? 16:00
A I think you've answered the question. Your 16:00
hypothesis is that if this is changed in the field, 16:00
the area doesn't change. 16:00
Is that your hypothesis? 16:00
Q No, sir. 16:00
I'm simply asking you: What is the size of 16:00
this driver circuit 300? 16:00
MR. RUECKHEIM: Object to the form. 16:00
THE WITNESS: The drive -- the size of 16:00
circuit 300 is the size of the circuit on the die. 16:00
And that size may be different from die to die if you 16:00
could change the circuit from die to die at design 16:00
time. 16:00
MR. TEZYAN: Okay. 16:01

Q Well, if we assume that driver circuit 300 is fixed in area, and just one or both of these enable 0, enable 1 drivers can be enabled or disabled, what would be your answer? 16:01
MR. RUECKHEIM: Object to the form. 16:01
THE WITNESS: I'm not sure what the question is. But I think the question is, what's the size of the driver 300? Is that your question? 16:01
MR. TEZYAN: Let me put the question in another way. 16:01
Q If the size of driver 300 is fixed in area, does the driver size depend on whether either of these enable 0 and enable 1 drivers is enabled or disabled? 16:02
MR. RUECKHEIM: Object to the form. 16:02
THE WITNESS: The driver size on the die that's fixed is the dimension of the -- of that driver. And the reason that it's a fixed dimension when you can enable one or the other is that the driver size has to be fixed to accommodate the worst-case power dissipation. 16:02
If you design it for enable 0 only, and then you drive it with both enable 0 and enable 1 driven -- driving it, you can burn up the chip. So you design for the worst case. 16:02
And therefore, you design for having enable 0 16:02

and enable 1 on if that could ever happen. That's the size of the -- the driver 300. 16:02
MR. TEZYAN: Okay. 16:02
Q So let's say driver 300 is X at fabrication; right? 16:02
If both enable 0 and enable 1 are on, the driver size is still X; right? 16:03
A The driver size is the physical area. And by enabling one or both of those drivers, you don't change that physical area. So the driver size is fixed. 16:03
Q So the answer to my question would be "yes"? 16:03
MR. RUECKHEIM: Object to the form. 16:03
THE WITNESS: Is there a question pending? I don't -- 16:03
MR. TEZYAN: Q. Well, the question was that if we say driver 300 has an area X, if enable 0 and enable 1 are both on, the driver size is still X; right? 16:03
A That's correct. 16:03
Q Okay. And if enable 0 is on but enable 1 is off, the driver size is still X; right? 16:04
A That's correct. 16:04
Q Okay. And if vice versa, enable 1 is on but enable 0 is off, driver size is still X? 16:04

A That's correct. 16:04
Q Understood. 16:04
Okay. I think we can take a break. 16:04
THE VIDEOGRAPHER: We are going to go off the record. The time is 4:04 p.m. 16:04
And it's the end of Media Unit No. 7. 16:04
(Recess taken.) 16:04
THE VIDEOGRAPHER: We are going back on the record. The time is 4:17 p.m. 16:17
And this is the start of Media Unit No. 8. 16:17
MR. TEZYAN: Welcome back, Dr. Stone. 16:17
Q Did you have any communications with your counsel during the break? 16:17
A I did not. 16:17
Q Dr. Stone, the earliest of the patents you analyzed has a priority date that goes back to 2007; right? 16:17
A I believe so. I -- I -- that sounds right. 16:17
Q Okay. So earlier, I asked you about the distinction between the term "rank" and the term "bank." I believe I asked 2006, but, you know, circa 2006-2007. 16:17
Do you recall that discussion? 16:17
A I do. 16:17
MR. TEZYAN: Okay. I think if you refresh 16:17

your Exhibit Share, you'll see I've marked Exhibit No. 14. 16:17
(Document remotely marked Exhibit 14 for identification.) 16:18
MR. TEZYAN: Q. Let me know when you have it, please. 16:18
A I see it now. 16:18
Q Okay. And Exhibit No. 14 is a document -- 16:18
A Let me do that. 16:18
Q Oh, go ahead. Sorry. 16:18
A I have it now on my screen. 16:19
Q Okay. And this is a document titled: "Frequently Asked Questions." 16:19
Right? 16:19
A That's correct. 16:19
Q And on the bottom -- you can see on the bottom of page 2, there is the Micron logo; correct? 16:19
A That's correct. 16:19
Q And it says "crucial.com"; right? 16:19
A That's correct. 16:19
Q And Crucial is a Micron brand; right? 16:19
A Say that question again. 16:19
Q Crucial is a Micron brand; right? 16:19
A I'm not aware. 16:19
Q Okay. So on page 2 where it says: 16:19

"What is the difference between a 'bank' and a 'rank'?" 16:19
Do you see that? 16:19
A I see that. 16:19
Q And it distinguishes between the term "bank" and the term "rank" by saying: 16:19
"Banks are specific to individual DRAM components and refer to sub-arrays within the DRAM component. Ranks are specific to memory modules and refer to a sub-array made of multiple DRAM components." 16:19
Right? 16:20
A I see that. 16:20
Q Okay. And so my question is: Does this distinction -- let me withdraw. 16:20
And I'll ask: Would a person of ordinary skill in the art have been aware of this distinction between bank and rank? 16:20
MR. RUECKHEIM: Object to the form, and beyond the scope. 16:20
THE WITNESS: Yeah, I need to know the date. 16:20
MR. TEZYAN: Q. You know, I don't know if this document has a date. 16:20
A It does. It's 2023 copyright. Okay. 16:20
So in 2023, a person of ordinary skill in the art would know the difference between bank and rank. 16:20

Q Okay. But is it your testimony that in 2007, a person of ordinary skill in the art would not have known this distinction? 16:20
A I haven't justified that. I don't know the answer. 16:21
Q Okay. Well, here, it says that ranks are specific to DRAM components; is that fair? 16:21
MR. RUECKHEIM: Object to the form. 16:21
THE WITNESS: That's not fair. 16:21
MR. TEZYAN: Okay. 16:21
Q Why not? 16:21
A In my book, I talk about how to build SRAM memories and also DRAM memories, and I have banks for both. And so at the time that I wrote the book in 1982, a bank would apply just as equally to a static RAM as it would to a dynamic RAM. 16:21
(Document remotely marked Exhibit 15 for identification.) 16:22
MR. TEZYAN: Q. Dr. Stone, could you please refresh your Exhibit Share. 16:22
A Sure. 16:22
Q I've marked Exhibit 15. 16:22
A We have Exhibit 15; is that correct? 16:23
Q Yes, sir. 16:23

A I'm uploading it. Just one moment. 16:23
I have now opened Exhibit 15 in my PDF reader. 16:23
Q Okay. Exhibit 15 is titled: 16:23
"Synchronous DRAM Architectures, Organizations, and Alternative Technologies." 16:23
Right? 16:23
A That's correct. 16:23
Q Okay. And the date of this paper is December 10th, 2002; right? 16:23
A That's correct. 16:23
Q Okay. Let's jump to page 2, please. 16:24
A I haven't read this document. May I have a moment? 16:24
Q Yeah, certainly. 16:24
A (Reading document.) 16:24
Okay. What I'd like to say is I have scanned this article. I'm generally familiar with the technology, but the details are very dense and extensive. 16:27
I'll do my best to answer the questions, but I reserve the right to say, I'm sorry. I just haven't studied this carefully. 16:28
Q Fair enough. 16:28
So on page 2, it says that: 16:28

"The term 'DRAM' stands for dynamic random access memory." 16:28
Do you see that? 16:28
A I see that. 16:28
Q And it says: 16:28
"It is characterized as 'dynamic' primarily because the values held in the memory array's storage cells are represented by small electric charges that slowly leak out of the circuit over time." 16:28
Right? 16:28
A I see that. 16:28
Q Okay. So DRAM -- I'm sorry. Let me rephrase the question. 16:28
A person of ordinary skill in the art would understand that DRAM has memory cells; right? 16:28
MR. RUECKHEIM: Object to the form, and beyond the scope. 16:28
THE WITNESS: I'm sorry. Repeat your question, please. 16:29
MR. TEZYAN: Certainly. 16:29
Q So a person of ordinary skill in the art would understand that DRAM has memory cells; right? 16:29
MR. RUECKHEIM: Same objection. 16:29
THE WITNESS: I'm sorry. I can't follow your words. "DRAM has," and then it got garbled. 16:29

MR. TEZYAN: I'm sorry. I'll try to speak clearer. 16:29
Q So a person of ordinary skill in the art would understand that DRAM has memory cells; right? 16:29
MR. RUECKHEIM: Same objection. 16:29
THE WITNESS: Are you saying DRAM has memory cells? You're swallowing that word. 16:29
MR. TEZYAN: Yes. 16:29
THE WITNESS: It has memory cells. 16:29
MR. TEZYAN: Q. And specifically, the smallest unit within a DRAM is a memory cell; right? 16:29
A I don't agree with that particularly. Where do you see -- is that in this article? 16:29
Q Yes. So if you'd scroll up to the figure that's immediately above this paragraph. 16:30
A Okay. Well, that -- that picture, it -- it destroys your argument. That -- the smallest item in the -- in this particular thing is not the storage cell. It's either the transistor or the capacitor. 16:30
Q Fair enough. 16:30
But the -- the smallest unit of -- of memory is that storage cell that's comprised of the capacitor and transistor; fair? 16:30
MR. RUECKHEIM: Object to the form of the question; beyond the scope. 16:30

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THE WITNESS: In smallest -- I don't know how you're measuring smallest. Is that physical? Is it, as you say, strength? I -- I -- I don't know. 16:30
MR. TEZYAN: Okay. 16:30
Q Take a look at the second column on this page, and particularly in the middle of that first full paragraph. And -- and feel free to take a moment to read that paragraph to yourself, please, and let me know when you're done. 16:31
A (Reading document.) 16:31
I see that, yes. 16:31
Q Okay. So my question is, there's the sentence somewhere in the middle that says: 16:31
"Lastly, there is a chip-select network that connects from the memory controller to every DRAM in a rank (a separately addressable set of DRAMs)." 16:32
Do you see that? 16:32
A I do. 16:32
Q And so my question is: Would a person of ordinary skill in the art in 2002 have known that a rank specifically refers to a separately addressable set of DRAMs as opposed to other non-DRAM memory? 16:32
MR. RUECKHEIM: Object to the form, and beyond the scope. 16:32
THE WITNESS: If you -- I have to see how

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rank is used in the rest of this document, if you don't mind. The document may talk about it in different contexts. 16:32
MR. TEZYAN: Q. Yes, go ahead. 16:32
And let me direct you, for example, to page 4, and that's Footnote 3. So Footnote 3, for example, says: 16:32
"The number of banks within a rank is usually equal to the number of banks within a single DRAM device." 16:33
Do you see that? 16:33
A I'm looking at Footnote 3 on page 4; is that correct? 16:33
Q Yes, sir. 16:33
A Ask your question again. 16:33
Q So this is distinguishing bank from rank; correct? 16:33
A No. 16:33
Q In -- no? Why is that wrong? 16:33
A The word "usually" is in the front -- the first line of Footnote 3. I would say usually, it distinguishes bank from rank. But "usually" means not always. 16:33
Q Okay. Fair enough. 16:33
Let's go to the above-the-line text where

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Footnote 3's call number is. And this is the sentence that starts with: 16:34
"The first step in handling a read request is for the memory controller to decompose the provided data address into components that identify the appropriate rank within the memory system, the bank within that rank3, and the row and column inside the identified bank." 16:34
So this is distinguishing a rank of memory devices from a bank within one of those memory devices; fair? 16:34
MR. RUECKHEIM: Object to the form, and beyond the scope. 16:34
THE WITNESS: In this case, it does, but it doesn't mean that they're always the same. It says "typically" in the sec- -- in the third-to-last line, and it says "typically one or more address bits," but not necessarily. 16:34
MR. TEZYAN: Q. That sentence reads: 16:34
"The bank identifier is typically one or more address bits." 16:34
Right? 16:34
A That's what it says, but it doesn't say how many there are. It could be none. 16:34
Q Okay. Well, the previous sentence isn't 16:35

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referring to bank identifiers; right? 16:35
MR. RUECKHEIM: Object to the form. 16:35
THE WITNESS: All I'm saying is that if you have 0 address bits for bank identifier, then rank and bank will be the same. Unusual. Possible, yes. 16:35
MR. TEZYAN: Okay. 16:35
Q But fair to say that generally by 2002, a person of ordinary skill in the art would have understood bank and rank to be different terms; fair? 16:35
MR. RUECKHEIM: Object to the form; beyond the scope. 16:35
THE WITNESS: I believe that this is consistent with "generally," yes. 16:35
MR. TEZYAN: Okay. 16:35
Q So returning to page 2 and that sentence: 16:35
"Lastly, there is a chip-select network that connects from the memory controller to every DRAM in a rank (a separately addressable set of DRAMs)." 16:36
A I got lost. Where are you reading from? 16:36
Q This is the middle of page 2, the sentence that starts "Lastly" in the first full paragraph on the right column. 16:36
A Right column. Got it. 16:36
Q And he says: 16:36
"Lastly, there is a chip-select network that 16:36

connects from the memory controller to every DRAM in a rank (a separately addressable set of DRAMs)." 16:36
Do you see that? 16:36
A I do. I haven't confirmed that he's using bank and rank separately through the whole document. I don't know that's the case. 16:36
Q Yeah, go ahead. 16:36
A Okay. Go ahead and ask your question. 16:38
Q So my question is: Is it fair to say that by 2002, a person of ordinary skill in the art would understand the term "rank" to refer to a set of DRAMs? 16:38
MR. RUECKHEIM: Object to the form. 16:38
THE WITNESS: The issue I have is that this is the -- what they call extrinsic evidence. And based on this, a person of skill in the art may believe one thing. But with extrinsic evidence, there may be other documents that say the opposite. 16:38
This is not directly what is taught in the patent unless you can identify where it is in the patent. 16:38
So I -- I will say, based on this, the answer could be "yes," but it also could be "no" if I had access to the extrinsic evidence at the time. 16:38
MR. TEZYAN: Okay. 16:39
Q Are you aware of any extrinsic evidence from 16:39

2002 onwards where rank is used to refer to a set of non-DRAM devices? 16:39
A That was not a task that I was assigned, so I did not look into that. I do not at this -- as I sit here today, I do not know the answer to that question. 16:39
Q Do any of the documents referenced in your declaration use the term "rank" to refer to a set of non-DRAM memory devices? 16:39
A I will look at my -- I -- I didn't look for rank and -- and bank in the documents I cited in the -- in my declaration. So I don't know if the answer is "yes" or "no." 16:39
Q The question wasn't about bank. It was about non-DRAM memory devices. So I'll just go ahead and ask it again. 16:39
A Okay. Go ahead. 16:39
Q Do any of the documents referenced in your declaration use the term "rank" to refer to a set of non-DRAM memory devices? 16:40
MR. RUECKHEIM: Object to the form. 16:40
THE WITNESS: I actually didn't check on that. I don't know. I don't know the answer. 16:40
MR. TEZYAN: Q. Dr. Stone, how long have you been working in the memory industry? 16:40
A My first memory design with integrated 16:40

circuits was 1973 or 1974. And I continued with memory design through my retirement at IBM in 2001. 16:40
Subsequently, I've been engaged as an expert witness analyzing documents that involve memory design. 16:40
So I would say almost continually since 1973 or '74 I've been involved with memory design, either doing it myself or analysis of memory designs. 16:40
Q Okay. I think I'm about done, but there's just one set of questions I want to go back to to clarify, if I may. 16:41
Can we please go back to Exhibit 7. 16:41
A Okay. 16:42
Q I just have one clarifying question. 16:42
A I have it in front of me. 16:42
Q And could we go to paragraph 63, please. 16:42
A Let me confirm that I -- this is my -- Exhibit 7 is my declaration, I believe? Yes. 16:42
Q Yes, sir. It's your declaration in IPR2018-00363. 16:42
A Okay. And what -- and we're going to paragraph -- what paragraph? 16:42
Q 63. 16:42
A 53. 16:42
Q 63. So that's on PDF page 30. 16:42
A I have 63 on page 30, yes. 16:42

Q And earlier, we were discussing a series of hypotheticals where the memory controller may or may not experience certain load of the memory devices. 16:43
Do you recall that conversation? 16:43
A I do. 16:43
Q Okay. So I just want to clarify with this one specific example, just so I make sure I understand your testimony. 16:43
In this situation where there is the X, right, data path B is -- is disabled; right? 16:43
And if you want to confirm that, you can read -- 16:43
A I didn't see the figure you're talking about. 16:43
Q Oh, I'm sorry. So it's -- 16:43
A Figure 5; right? 16:43
Q Correct. It's Figure 5. 16:43
And you can read paragraph 64 if that will -- 16:43
A Okay. 16:43
Q -- help. 16:43
A And it's on page 31 that you're referring to? 16:43
Q Yes, sir. 16:43
A And I see the X. Now ask your question. 16:43
Q So my question is: The X indicates that data path B is disabled; right? 16:43
A That's correct. 16:44

Q Okay. So if data path B is disabled, how many loads will the memory controller see in this configuration? 16:44
MR. RUECKHEIM: Object to the form. 16:44
THE WITNESS: Memory controller 518? 16:44
MR. TEZYAN: Q. Memory controller is 420 on the bottom left. 16:44
A System Memory Controller; is that correct? 16:44
Q What's that? 16:44
A 420 you said to be System Memory Controller; is that correct? 16:44
Q Yes, sir. 16:44
And my question is: How many loads will the memory controller experience in this configuration? 16:44
Will it experience the loads of both Memory Ranks A and C, or will it experience only one load? 16:44
MR. RUECKHEIM: Object to the form. 16:44
THE WITNESS: The memory controller will experience at least the load of Y1. But the load on Y2 may be adjusted on line -- on -- on chip -- on chip changing the -- the resistor. That would be on die control of the load. 16:45
And so because Y2 is disabled, if they change the load on the driver 506, then the System Memory Controller may see something different. 16:45

But that go -- it actually goes through 518. 16:45
Are you asking what 518 sees or what, in this case, 420 sees? 16:45
MR. TEZYAN: Q. I'm asking what 420 sees. 16:45
A It sees the load from 518. I don't see how what's happening with the X changes the load that 518 presents to the controller. 16:45
Q 518, if you look at paragraph 64, is just the data line. 16:46
So maybe let me ask the question this way: Is it the load of 503 that the memory controller will experience? 16:46
MR. RUECKHEIM: Object to the form. 16:46
THE WITNESS: I have to -- I'm sorry. I have to make sure that 518 is what you say it is. 16:46
MR. TEZYAN: Yeah. 16:46
Q And that's paragraph 64. 16:46
A So your assumption is that D is -- has no active component in it; is that correct? 16:47
Q That's right. 16:47
A If it has no active component, now I understand more of your question. 16:47
And what is your question again? 16:47
Q My question is: In -- in this configuration where data is being driven along data path A from the 16:47

memory controller, is the load that the memory controller sees the load of 503? 16:47
MR. RUECKHEIM: Object to the form. 16:47
THE WITNESS: Well, the -- in both cases, it sees the load of 503. But that load may not be the same in both cases. 16:47
MR. TEZYAN: I'm sorry. 16:47
Q What's the second case? 16:47
A Well, you have a case where A is driving, and a case in another figure where the 506 is driving, B, and the -- or a case where neither of them are driving. 16:48
But the -- the load that 503 sees is not the sum of the loads on 504 and 506 if there is online die termination, because the online die termination can change the load of an inactive driver. 16:48
Q Okay. Would the load that the memory controller sees increase in the absence of 503? 16:48
MR. RUECKHEIM: Object to the form; beyond the scope. 16:48
THE WITNESS: In the absence of 503? 16:48
MR. TEZYAN: Yes, sir. 16:48
THE WITNESS: The memory controller is driving memory; right? 16:48
MR. TEZYAN: Yes, sir. 16:48

THE WITNESS: And you're asking me, you don't have 503 now that's driving memory? I don't know how that's possible.

MR. TEZYAN: Q. But 503 is a write buffer; correct, sir?

You can confirm that in paragraph 64.

A Okay. And you're asking me to leave out the write buffer; is that correct?

Q Well, let me ask you first: What does the write buffer do in this implementation?

MR. RUECKHEIM: Object to the form.

THE WITNESS: It could do one of two things. As a buffer, it -- it will receive in the -- regenerate. Another thing it can do is delay a clock time if it's clocked. It doesn't have to be clocked, but if it is clocked, it can delay.

MR. TEZYAN: Okay.

Q And the question is just: If we were to take this configuration in Figure 5 and remove write buffer 503, would the load that the memory controller sees increase or decrease?

MR. RUECKHEIM: Object to the form.

THE WITNESS: I can't tell from the figure.

Okay. Let me hypothesize that the load would be the same, because somehow by magic, online die

determination on Y2 is injected. So there is no load caused by 506. And the load of 504 is identical to the load of 503. In that case, there is no change.

That's hypothesis. I'm not saying that's what's going to happen.

Otherwise, I don't know what's going to happen. I have to see the numbers.

MR. TEZYAN: Q. Let's jump to paragraph 66, and maybe this can help clarify for me what's going on. So you write that:

"The '907 Patents' 'data transmission circuits 416 [(red box)]] present a load [to the memory controller 420] on the data lines 518 from the write buffer 503 and the read buffer 509 ... that is substantially the same as the load that one of the memory devices 412 would present."

Is that right?

A Just a moment.

That's a quote from the patent. So if you're asking me if that's what I put in there as a quote from the patent, that's what I put in there, yes.

Q Okay. Well, I'm asking: In the absence of that write buffer 503, would the load that the memory controller sees increase or decrease?

MR. RUECKHEIM: Object to the form.

THE WITNESS: I'm missing some context here. Just before Section D, the quote reads:

"That is substantially the same as the load that the memory controller 420 would present."

I'm trying to find 420 in these figures.

Oh, there it is. Now I got it. Okay. I got it.

Q Okay.

A I understand. Now you can ask your question, and I can answer it.

Q Okay. My question was: In the absence of that write buffer 503, would the load that the memory controller sees increase or decrease?

MR. RUECKHEIM: Object to the form.

THE WITNESS: Well, I'm not sure I can answer that question exactly.

But I am informed by this quote that the load presented by 503 is deliberately set to be what the system controller would see if there weren't the Y1, Y2, and things like that.

503 is designed to present a load similar to a memory cell. I'll show you where that is. Look at paragraph 66 at the beginning, and it says:

"Data transmission circuits 416" -- "present a load [to the memory" -- "controller" -- on the

lines -- on -- "data lines 518 from the write buffer 503 and the read buffer 509 ... that is substantially the same as the load that one of the memory devices" --

That's by design. Okay. The designer says, I know what the load is on memory, and I'm going to make that load on 503. And in going the reverse direction, the same holds true. I don't have to analyze that right now.

So you're asking a hypothetical which just -- I don't understand how that hy- -- hypothetical would -- would come into play.

Here, we have the situation -- I'm looking at the figure just above paragraph 64 -- where deliberate design makes the load 503 equal to the memory.

And you're saying, Take it out. What happens?

I don't know. I know that the designer wouldn't want to do that. Anything the designer would put in would try to make that load the same as the memory. But I don't know what's there.

MR. TEZYAN: Okay. Fair enough.

Q My question was just whether you know or not if taking out that write buffer 503 would increase or decrease the load.

For example, would you see the load of both of those memory devices A and C? 16:58
A I know that there are -- 16:58
MR. RUECKHEIM: Objection. 16:58
THE WITNESS: -- several possibilities. 16:58
Okay. If your -- I didn't mean to interrupt your question. Finish your question. 16:58
MR. TEZYAN: Q. No, sir. That was the question. Go ahead. 16:58
A Okay. I know that there are several possibilities, and they don't matter. 16:58
One possibility is the -- the on-chip termination. It makes the load of Y2 or Y1 the same as the memory. And then when you disable Y1 or Y2, you don't change a load. That's a possibility. Okay. 16:58
Another possibility is that there is still some load in Y1 and Y2, but the combined load is the same as the memory load. So whether the Y1 or Y2 is in tristate load, you fix the load so that the total load is the same as memory. 16:59
These are various possibilities. 16:59
MR. TEZYAN: Okay. Just a few final questions. 16:59
Q Dr. Stone, have you designed memory modules? 16:59
A I have. 16:59

Q What kind of memory modules? 16:59
A Well, one that -- that's in my book. But more -- let me tell you a story about how I did a design review and corrected a real problem. 16:59
If you look at my vitae, you'll see that I was a consultant to Sperry. Sperry made, at that time, navigation computers for the nuclear fleet -- 16:59
the strategic nuclear fleet. 16:59
They called me because they put a new navigation computer in a -- in a nuclear sub, sent it out for sea trials, and it failed sea trials. So they asked me to come. 17:00
I came, they showed me the board, and I knew what the problem was. I knew. Okay. So I didn't know how Sperry designed their memory boards for their personal computers. I had no idea. 17:00
I told the people there to bring me in a board designed for the personal computers, and they did. And so I -- for the first time in my life, I saw that board, and I compared it to the navigation computer board. I held them up. 17:00
I said, Look, they're different. And the reason that the failure occurred in the fleet is because the fleet navigation computer failed to follow the rules for designing memory. In fact, it failed to 17:00

follow the rules that I had in my book. 17:01
Q Can I ask where on your CV that is? 17:01
A Pardon me? 17:01
Q Can I ask where on your CV that's listed, sir? 17:01
A You should be looking at the -- I'll show you where. Chapter 4. I'll bring it up in a minute. I just have one more sentence to say. 17:01
They redesigned the board. It passed sea trials. 17:01
Okay. Let's show you where it is. 17:01
Q Well, I can just cut to the chase and ask my question: What year was that, sir? 17:01
A What year? The year I did this was 1984, 1985, something on that -- or '83, '84, '85. 17:01
Q Okay. So have you ever designed DDR memory modules? 17:01
A I have. 17:01
Q When? 17:01
A When did I do that? 17:01
I was engaged in the design of a memory for the IBM Power PC, and I was on the design team for that memory. So I personally didn't lay out the memory design, but I did this while I was working at IBM 1982, '83. And that was DDR memory, an early 17:01

version of it. 17:02
I'm sorry. I got the wrong year. 1992 to 1993. 17:02
Q Okay. But fair to say you've never designed, you know, DDR4 memory modules? 17:02
A I have never designed DDR4 memory modules. That is correct. 17:02
Q Okay. And the same with DDR5 memory modules, I take it? 17:02
A I have never designed DDR5 memory modules. 17:02
Q And just a quick follow-up question on the load reduction issues we were discussing a moment ago. You said with on-die termination, the load on path A or path B would change; correct? 17:02
A That's what my testimony was, yeah. On-die termination changes how waves react when they touch a device. 17:03
Q Okay. So would the memory controller see more than one load if the write buffer 503 is not there? 17:03
MR. RUECKHEIM: Object to the form. 17:03
THE WITNESS: I -- I have a lot of problems with that. The load can be expressed as the impedance -- the input impedance of Y2, or it can be expressed in another way. So I'm not sure what you 17:03

mean by "load." 17:03
MR. TEZYAN: Q. Let's -- let's start with 17:03
capacitive load. 17:03
A Capacitive load? 17:03
Q Uh-huh. So I'll just reframe my question 17:03
then. 17:04
A Okay. 17:04
Q So would the memory controller see more than 17:04
one capacitive load if the write buffer 503 is not 17:04
there? 17:04
MR. RUECKHEIM: Object to the form. 17:04
THE WITNESS: If 503 is not there, there will 17:04
be capacitive load on the conductor that goes from 518 17:04
to one of the Y2s and Y1s. It would see capacitive 17:04
load. And that could be about the same as if 503 is 17:04
there, or it could be more if 503 is there -- I'm 17:04
sorry. 17:04
I don't -- putting 503 in the loop may or may 17:04
not increase the capacitive load, be- -- because the 17:04
lines may have to be rerouted to go to 503 before they 17:04
go to Y2, and they can be shorter if they go directly 17:04
to Y2. Okay. 17:04
So I don't know how the capacitors change 17:04
when you take 503 in or out. You talk -- I can't 17:05
tell. 17:05

MR. TEZYAN: Okay. 17:05
Q But assuming the lines are the same length, 17:05
would the capacitive load change? 17:05
MR. RUECKHEIM: Object to the form. 17:05
THE WITNESS: To the extent that the 17:05
capacitive load is determined by that particular line, 17:05
if the line is the same length, it won't change. 17:05
MR. TEZYAN: Right. 17:05
Q But what I'm saying is, you're saying, and 17:05
correct me if I'm wrong, that it depends in part on 17:05
whether if you take that write buffer out, and you 17:05
also swap the -- the length of that line. 17:05
Is that what you're saying? 17:05
A I'm saying that the capacitive load depends 17:05
on the length of the connection between D and Y2. And 17:05
if you put 503 in and out, that length can increase or 17:05
can decrease. And so I can't tell you if the 17:05
capacitive load is bigger, smaller, or equal. 17:05
Q Okay. And what I'm saying is, if you just 17:05
take 503 out, and you don't change the length of that 17:05
connection between D and Y1, does the capacitive load 17:06
change? 17:06
MR. RUECKHEIM: Objection. 17:06
THE WITNESS: If you don't -- okay. If you 17:06
take 503 out, you'll probably change the capacitive 17:06

load by reducing the length in line, because you don't 17:06
have to visit 503. 17:06
So if you insist on writing -- routing a line 17:06
to a place where 503 might have been, then rerouting 17:06
it to Y2 so that the line length is the same, yeah, 17:06
the capacitive load will be the same. But it doesn't 17:06
have to be that way. 17:06
MR. TEZYAN: Okay. 17:06
Q So would the load that the memory controller 17:06
sees increase if the write buffer 503 is not there or 17:06
decrease -- 17:06
MR. RUECKHEIM: Object to the form. 17:06
MR. TEZYAN: Q. -- all else being equal? 17:06
A I think I've answered that question. The 17:06
answer is, you can't tell, because I don't know the 17:06
length of the line that you're actually going to put 17:06
in. 17:06
I know that your hypothesis says that the 17:06
line length is the same. I'm saying, Oh, okay. The 17:06
capacitance will be the same. 17:07
I don't think that's what's going to happen. 17:07
So your -- your hypothetical may not be true. And 17:07
what is true is the line length may be longer, equal, 17:07
or shorter, and that's what the situation is. 17:07
MR. TEZYAN: Okay. Pass the witness. 17:07

MR. RUECKHEIM: Let's take a ten-minute 17:07
break. 17:07
THE WITNESS: Okay. 17:07
THE VIDEOGRAPHER: We're going to go off the 17:07
record. The time is 5:07 p.m. 17:07
And it's the end of Media Unit No. 8. 17:07
(Recess taken.) 17:08
THE VIDEOGRAPHER: We are going back on the 17:19
record. The time is 5:19 p.m. 17:19
And this is the start of Media Unit No. 9. 17:19
17:19
EXAMINATION 17:19
BY MR. RUECKHEIM: 17:19
Q Hello, Dr. Stone. 17:19
A Hello. 17:19
Q If you can turn to Exhibit 1, which was your 17:19
declaration. 17:19
A I have it. 17:20
Q Okay. The declaration you submitted in this 17:20
case involved which U.S. patents? 17:20
A I think I have a list of them. It involved 17:20
the '060 and the '160, and also involved the '9 -- 17:20
there it is -- '918 and the '054. 17:20
Q And if you can turn to -- starting around at 17:20
the bottom of page 7 of your declaration. 17:20

A Okay. Give me a minute. 17:20
I'm at page 7 at the bottom. 17:21
Q Okay. And did you provide opinions as to 17:21
what would constitute the level of ordinary skill in 17:21
the art for the patents you just mentioned? 17:21
A I did. 17:21
Q And did you apply those -- those levels of 17:21
ordinary skill in coming up with your opinions? 17:21
A I did. 17:21
Q Did you provide opinions as to what would 17:21
constitute a person of ordinary skill in the art with 17:21
respect to any other patents? 17:21
A Well, this is just the '060 and '160. I did 17:21
one for the '918 and the '054. That's on page 8. 17:21
Q And did you provide opinions as to what would 17:21
constitute a person of ordinary skill's knowledge with 17:21
respect to any other patents in your declaration? 17:21
A I did not. 17:21
MR. RUECKHEIM: Thank you. 17:21
No further questions. 17:21
MR. TEZYAN: I have some follow-up questions. 17:21
17:21
FURTHER EXAMINATION 17:21
BY MR. TEZYAN: 17:21
Q Dr. Stone, while we're on paragraph 23, you 17:21

Q You testified earlier that in preparation for 17:23
this deposition, you reviewed the parties' briefs in 17:23
this case; is that right? 17:24
A I reviewed the parties' briefs. Yeah, I did 17:24
that. 17:24
Q And those briefs include arguments for the 17:24
'506 patent; is that right? 17:24
A I'd have to look. I believe that's the case, 17:24
but I -- may I confirm? 17:24
Q Yes, sir. 17:24
A And the patent number was, what, '506? 17:24
Q Yes, sir. 17:24
A I have confirmed that the '506 is discussed 17:24
in the brief from Netlist. 17:24
Q And those briefs also include argument for 17:24
the '339 patent; right? 17:25
MR. RUECKHEIM: Object to the form. 17:25
THE WITNESS: Okay. Let's see. 17:25
MR. TEZYAN: Q. That's the one that 17:25
discusses fork in the road. 17:25
A Yes. I -- I'm just checking to verify that 17:25
it's in this. 17:25
It did. It's -- it is discussed in the 17:25
Netlist brief. 17:25
Q And is it fair to say that the subject matter 17:25

say that a hypothetical person would have been 17:22
familiar with the JEDEC industry standards, 17:22
knowledgeable about design and operation of SDRAM -- 17:22
sorry -- DRAM and SDRAM memory devices and memory 17:22
modules, and going on, such a hypothetical person 17:22
would have been familiar with the structure and 17:22
operation of circuitry used in stacked memory devices; 17:22
right? 17:22
A That's correct. 17:22
Q And would have been familiar with components 17:22
including ASICs, FPGAs, CPLDs, and low-level circuits 17:22
such as tristate buffers; right? 17:22
A Are you asking, did I see that? Or what's 17:22
your question? 17:22
Q I'm asking if you see that. 17:22
A I see that, and I did that. 17:22
Q Okay. And in paragraph 25, you provide a 17:22
substantially similar explanation for what you believe 17:22
a person of ordinary skill in the art at the time of 17:22
these inventions would have known; is that fair? 17:22
A That's fair. That's correct. 17:22
Q And you also testified that in preparing for 17:23
this deposition, you reviewed the parties' briefs in 17:23
this case; right? 17:23
A Repeat your question, please. 17:23

of the '506 and '339 patent are similar to the subject 17:25
matter of the '918, '054, '160, and '060 patents? 17:25
MR. RUECKHEIM: Object to the form. 17:25
THE WITNESS: The patents are different. And 17:25
similarity, I don't know what's in your mind. I know 17:25
the claims are different, and there is some technology 17:25
that's similar. 17:25
I can't answer your question as asked without 17:25
understanding it better. 17:25
MR. TEZYAN: Okay. Fair enough. 17:25
Q But a person of ordinary skill in the art in 17:26
the '339 and '506 patents would have had some common 17:26
knowledge as a person of ordinary skill in the art 17:26
with the '918 and '054 patents, let's say? 17:26
MR. RUECKHEIM: Objection to form. 17:26
THE WITNESS: I'm just checking to see if 17:26
they're incorporated by reference. I -- I haven't 17:26
looked everywhere, but I don't see where they're 17:26
incorporated by reference into the patents I looked 17:26
at. But let me check a little further. 17:26
MR. TEZYAN: I don't believe that's 17:27
necessary. Let me just rephrase my question. 17:27
Q As an example, is it fair to say that the 17:27
'060 and '160 patents are directed to load reduction 17:27
for a memory product? 17:27

MR. RUECKHEIM: Object to the form. 17:27
THE WITNESS: It is fair to say that they 17:27
are -- address loads and load reduction, yes. 17:27
MR. TEZYAN: Okay. 17:27
Q And is it fair to say that the '339 patent is 17:27
generally directed to load reduction? 17:27
MR. RUECKHEIM: Object to the form. 17:27
THE WITNESS: Possibly. I mean, I -- I'd 17:27
need to bring up the '339 again. 17:27
MR. TEZYAN: Okay. 17:27
Q Give me one second, and I'll bring it up for 17:27
you. 17:27
A Okay. 17:27
Q And to be clear, have you reviewed the 17:27
'339 patent? 17:27
A Not for this deposition. I'm -- I've 17:27
reviewed things like it before, and I think you have 17:27
an IPR where there is a patentee of the '339 or a 17:27
family member. So I'm familiar with it there, yes. 17:28
MR. TEZYAN: Okay. Just give me a minute. 17:28
Okay. If you'll go in the marked exhibits 17:28
folder, you'll see I've uploaded a new exhibit. 17:28
(Document remotely marked Exhibit 16 17:28
for identification.) 17:28
THE WITNESS: Okay. I'm refreshing now. I 17:28

see the '339 patent is in the folder, and I'm 17:28
downloading it. 17:29
I have now uploaded it. It's in my reader. 17:29
MR. TEZYAN: Okay. 17:29
Q And just to confirm, what will be marked as 17:29
Exhibit 16 is U.S. Patent No. 10,949,339; is that 17:29
correct? 17:29
A That is correct. 17:29
Q Okay. So please take a minute to review it, 17:29
and let me know when you're done. 17:29
A Okay. Ask your question, please. 17:31
Q So my question was: Is it fair to say that 17:31
the '339 patent is generally directed to load 17:31
reduction? 17:31
MR. RUECKHEIM: Object to the form. 17:31
THE WITNESS: I searched for the word 17:31
"load" and "reduction." I didn't see that. It could 17:31
be directed to other things besides load reduction, as 17:31
my understanding goes. 17:32
MR. TEZYAN: Q. Well, let's go ahead and 17:32
look at the Abstract, for instance; right? 17:32
A Okay. 17:32
Q So the Abstract says that: 17:32
"The memory module comprises DDR DRAM devices 17:32
arranged in multiple ranks." 17:32

Right? 17:32
A Yes. 17:32
Q So the '339 patent is directed to, in part, 17:32
at least DDR memory modules with ranks comprising DRAM 17:32
devices; is that fair? 17:32
MR. RUECKHEIM: Object to the form. 17:32
THE WITNESS: It is -- it describes "DDR DRAM 17:32
devices arranged in multiple ranks." Yes, that is 17:32
true. 17:32
MR. TEZYAN: Okay. 17:32
Q And if we go to column 6, line 61, you see 17:33
the sentence that says: 17:33
"In addition, as with the memory subsystems 17:33
100, 100' of FIGS. 1A and 1B, the 'fly-by' memory 17:33
subsystems 200, 200' of FIGS. 2A and 2B suffer from 17:33
large loads which result in slower clock speeds." 17:33
Do you see that sentence? 17:33
A I do. 17:33
Q So at least one of the problems that the 17:33
'339 patent identifies is large loads; is that fair? 17:33
A I don't believe so. 17:33
MR. RUECKHEIM: Object to the form. 17:33
MR. TEZYAN: Q. I'm sorry. I didn't get 17:33
your answer, sir. 17:33
A I -- I don't think that's the case. 17:33

Q Why is that? 17:34
A It is directed to adjusting timing, and 17:34
timing may be due to loads or other things. So at 17:34
least what I read from the paragraph that you just 17:34
quoted, that it is directed to timing. 17:34
Q Okay. Fair enough. 17:34
Let me direct your attention to column 7, 17:34
line 44. 17:34
A Okay. Okay. Line 44. I see it. 17:34
Q And Figure 3 -- it says that: 17:34
"FIG. 3A schematically illustrates an example 17:34
memory subsystem 400 with loadreduced memory modules 17:34
402 in accordance with certain embodiments described 17:34
herein." 17:34
Do you see that? 17:34
A I do. 17:34
Q Okay. So it's fair to say that at least some 17:34
embodiments of the invention of the '339 patent are 17:34
directed to load reduction -- 17:35
MR. RUECKHEIM: Object to the form. 17:35
MR. TEZYAN: Q. -- right? 17:35
A To say that it's directed to load reduction, 17:35
I think, is putting the cart before the horse. It is 17:35
directed to memory timing, and one way to deal with 17:35
memory timing is to reduce load. 17:35

I don't know that I would say that they're going to reduce load and not adjust the timing. I believe that the important thing is getting the timing adjusted. 17:35

Q Okay. But Figure 3A is literally a loadreduced memory module; fair? 17:35

A That's correct. That is correct. 17:35

Q Okay. So one solution to the problem that this patent identifies is the loadreduced memory module that's identified in Figure 3A; right? 17:35

MR. RUECKHEIM: Object to the form. 17:35

THE WITNESS: That's not the whole solution. That contributes to the solution, but there are other things that contribute to that solution. 17:35 17:36

MR. TEZYAN: Okay. 17:36

Q How does the '339 patent achieve that load reduction solution? 17:36

MR. RUECKHEIM: Object to the form. 17:36

MR. TEZYAN: Q. And if you want to go back to Figure 5 or reference any of the disclosures, go ahead. 17:36 17:36

A It's okay. I'm looking. Okay. 17:36

The best answer I can give in this is on page -- on column 6 at the very bottom. It describes how one deals with fly-by configurations, and that 17:38 17:38

fly-by configurations have been useful to correct timing problems. 17:38 17:38

And -- and it says that there has been a recent suggestion to provide a memory buffer which handles both the control signals and the data signals. And so it describes a way to use a data buffer to correct issues with fly-by that you try to use unsuccessfully. 17:38 17:38 17:38 17:39 17:39

It does say that fly-by is corrupted by load, but it does also say that it's going to use fly-by in conjunction with a memory buffer to handle both control and data signals. 17:39 17:39 17:39

So these are various techniques it's using. 17:39

Q Sorry. I was muted. 17:39

My question was: Figure 5 of the '339 patent is an example of one of those memory buffers in accordance with the invention; right? 17:39 17:39 17:39

MR. RUECKHEIM: Object to the form. 17:39

THE WITNESS: That's -- that's correct. 17:39

MR. TEZYAN: Okay. 17:39

Q So how does Figure 5 go about reducing the load that the memory controller sees? 17:39 17:39

MR. RUECKHEIM: Same objection. 17:39

THE WITNESS: In Figure 5, let's go to -- in Figure 5, let's talk about doing -- sending commands 17:39 17:40

or write data from 420 to the memory cells. 17:40

The memory of 420 in the absence of the circuitry we see in Figure 5 would see the load of a memory cell, let's say the load of 452 or something. 17:40 17:40 17:40

And what has happened is the designer has made 503 have a load that is essentially the same as what the 420 memory controller would see if there weren't this intermediate circuitry. 17:40 17:40 17:40

So, I mean, that's -- that's really the basis. I think I've answered your question. 17:40 17:40

MR. TEZYAN: Okay. 17:40

Q And in a read operation, how would the circuitry reduce the load that would otherwise be experienced? 17:40 17:40 17:41

A Okay. This is going the other direction. 17:41

MR. RUECKHEIM: Objection. 17:41

Go ahead. 17:41

THE WITNESS: Sorry. Finish. Would you repeat. I -- I -- I stepped over you. Go ahead. You want to repeat your answer -- 17:41 17:41 17:41

MR. TEZYAN: I will repeat the question, and then Mr. Rueckheim can repeat his objection if he wants to. 17:41 17:41 17:41

Q So the question is: In a read operation, how would the circuitry reduce the load that would otherwise be experienced? 17:41 17:41 17:41

MR. RUECKHEIM: Same objection. 17:41

THE WITNESS: Okay. You have the quote that I inserted into my declaration. The quote said, going in the direction from memory to 420, the circuitry is designed so that the memory cells see a load as if they were driving 420. 17:41 17:41 17:41 17:41 17:41 17:41

Let me pull up my -- where I said that in my report. 17:41 17:41

MR. TEZYAN: Q. I believe that was paragraph 66 of Exhibit 7. 17:41 17:42 17:42

A Yes, I -- I got it. I'm reading 65: 17:42

"For a read operation, the data transmission circuit 416 [(red box)] operates as a multiplexing circuit. In the illustrated embodiment of Fig. 5, for example, data signals read from the memory devices 412 of a rank are received at the first or second terminals" -- 17:42 17:42 17:42 17:42 17:42 17:42 17:42 17:42 17:42 17:42

Et cetera. 17:42

And then it says later on at -- at paragraph 66 at the bottom, it says: 17:42 17:42 17:43

"Similarly, the data transmission circuits 416 [(red box)]] present a load [to the memory devices 412] on the first and second terminals Y1, Y2" -- 17:43 17:43 17:43 17:43

Okay. So there is a deliberate design to 17:43

make the memory circuits see a load that's the same as they would see if they were the -- driving the memory controller 420. 17:43

And this quote ends with the phrase: 17:43

"That is substantially the same as the load that the memory controller 420 would present." 17:43

So the way they're doing with load is to imitate the load you would see if you didn't have these devices present. 17:43

Q Okay. And just to make sure I understand, in a read operation, what is the role that read buffer 509 plays in reducing the load? 17:44

MR. RUECKHEIM: Object to the form; well beyond the scope of the redirect. 17:44

THE WITNESS: Are you asking me -- now, I'm looking at the annotated figure on page 31 of my report. I'm sorry. Yes. Page -- 17:44

MR. TEZYAN: Yeah. 17:44

Q You can look at that one, or you can look at the '339 patent. 17:44

A Okay. And you're asking what role the driver 509 plays. The 509 driver is the driver that's driving the system memory. That's its role. 17:44

Q How does it contribute to load reduction for a read operation? 17:45

I think that's -- that's my question. 17:45

MR. RUECKHEIM: Same objections. 17:45

THE WITNESS: It's isolated. I -- I -- the memory -- the key thing here is the load that the memory sees. And the memory sees the load from Y1 or Y2 which may be less than it would see if it had to drive system memory and all the other -- all the other modules that share the bus. The memory only sees Y1. 17:45

And the contribution of 509 to that, it doesn't really change the load. The contribution is from the fork in the road. 509 drives the system that way. That's its role. 17:45

MR. TEZYAN: Okay. 17:45

Q So in the absence of 509, the load experienced by the memory devices in a read operation would stay the same. 17:45

Is that what you're saying? 17:45

MR. RUECKHEIM: Object to the form; beyond the scope. 17:46

THE WITNESS: The load experienced by memory in the absence of all that circuitry would be the load presented by the system memory controller and the load presented by other modules that share the bus. 17:46

MR. TEZYAN: Q. What do you mean by "all that circuitry," sir? 17:46

MR. RUECKHEIM: Same objections. 17:46

THE WITNESS: It's the circuitry that is put in between the memory ranks in 518D. It's the circuitry that does the fork in the road, if you wish, something like that. 17:46

MR. TEZYAN: Okay. Understood. 17:46

Q So you're saying essentially in the absence of a data buffer, the load experienced by the memory would be the load presented by the system memory controller and the load presented by the other modules that share the bus. 17:46

Do I have that right? 17:47

A That's correct. 17:47

MR. RUECKHEIM: Same objections. 17:47

MR. TEZYAN: Okay. 17:47

Q And then I guess my more specific question was, say you keep that circuitry intact, right, but you take out read buffer 509. 17:47

For a read operation, does that affect the load that the memory devices experience? 17:47

MR. RUECKHEIM: Same objections. 17:47

THE WITNESS: My belief is that it does, but I can't tell with certainty because we don't have enough detail. 17:47

The reason I believe it does is that 509 is 17:47

isolated from Y2 by these -- by 508. So I can't tell if you take out Y2 and 508 -- I'm sorry. 17:47

What are you taking out? 17:48

MR. TEZYAN: Let me clarify. 17:48

Q So you're just taking out 509. 17:48

And my question is: If you just take out 509, does the load that's experienced by a memory device in this system change as a result? 17:48

MR. RUECKHEIM: Same objections. 17:48

THE WITNESS: Okay. You're going to take out 509, but still have Y2 and Y1? 17:48

MR. TEZYAN: Uh-huh. 17:48

THE WITNESS: Is that correct? 17:48

MR. TEZYAN: Yes, sir. 17:48

THE WITNESS: The load experienced by the memory is the load presented by Y1 and Y2. 509 has no impact on that. 17:48

MR. TEZYAN: Q. And in a write operation, if you were to take out 503, leaving everything else the same, would the load on the memory controller change? 17:48

MR. RUECKHEIM: Same objections. 17:48

THE WITNESS: We discussed this earlier because of the complexity. And you're telling me that you're going to leave everything else the same, but you're taking out 503. And I just -- it's hard for me 17:49

to fathom that, because you don't have to route your wires to 503. Okay. 17:49
But if you're going to insist that all the capacitance stays the same, if you take out 503, probably the capacitance would increase without 503, probably, but not necessarily. And so the load would increase. 17:49
But if you can actually shorten the line between 518 and Y2 and Y1 because 503 is not present, it doesn't necessarily follow that capacitance of the load would increase. 17:49
MR. TEZYAN: Okay. 17:49
Q But you say that the load would -- that capacitance would probably increase. 17:50
Why -- why do you think it would probably increase? 17:50
MR. RUECKHEIM: Same objections. 17:50
THE WITNESS: I -- if you are trying to connect D and Y2, and you have to go through an intermediate spot, you lose the ability to go directly from D to Y2. Okay. If you can't go directly, you probably have a longer path. That's why I say that. 17:50
Did I answer your question? 17:50
MR. TEZYAN: I don't think so. So let me see if I can go back to your testimony. 17:50

Q So you said if you take out 503, probably the capacitance would increase without 503; right? 17:50
A That's correct. 17:50
Q Okay. And I'm asking why you think that's the case. 17:50
MR. RUECKHEIM: Same objections. 17:51
THE WITNESS: Okay. Look at it geometrically. D is a point. Y is a point. There is a straight line that could connect D to Y. It has a certain length. 17:51
Now, 503 is another point. If I drew a straight line from D to 503, and it did not lie in the path between D and Y1 directly, and then I connected 503 to Y1, the length of the path from D to 503 to Y1 would be longer than the direct path from D to Y1. 17:51
And you're telling me that you would take out 503 and not change the path. 17:51
I'm saying that A, if you're going to take out 503, I'm going to make the path direct, as direct as I can. I will shorten the path. And that's why I believe it's realistic to assume that the capacitance would be lower. 17:51
MR. TEZYAN: Okay. 17:51
Q But assuming you don't change the size of the path, then the capacitance would be the same or 17:52

higher? 17:52
MR. RUECKHEIM: Same objections. 17:52
THE WITNESS: Okay. If you don't change the length of the path -- I'm sorry. 17:52
If you leave the path alone, the way it is, you take out 503, the path between D through the 503 removal and then on to Y2 would probably be longer than the path from D to 503. Possibly. 17:52
So it might be the case that removing 503 and leaving all the other path lengths alone, you increase the capacitance. Therefore, you increase the load. 17:52
MR. TEZYAN: Okay. I have no further questions, pending questions from Micron counsel. 17:53
MR. RUECKHEIM: No questions from Micron. 17:53
MR. TEZYAN: Okay. 17:53
MR. RUECKHEIM: We're done. 17:53
MR. TEZYAN: We can go off the record. 17:53
STENOGRAPHIC REPORTER: Do you both need a copy? 17:53
MR. RUECKHEIM: Yes. 17:53
MR. TEZYAN: Yeah. 17:53
First, Dr. Stone, thank you very much. I appreciate your time. 17:53
THE WITNESS: You're welcome. You're welcome. 17:53

MR. TEZYAN: All right. You can hop off now. 17:53
THE VIDEOGRAPHER: Is there anything further? 17:53
MR. TEZYAN: What's that? 17:53
THE VIDEOGRAPHER: Counsel, do you want to go off the record? 17:53
MR. TEZYAN: Yeah, yeah, yeah. 17:53
THE VIDEOGRAPHER: Okay. If there is nothing further, we are off the record at 5:53 p.m. Pacific Daylight Time. And this concludes today's testimony given by Dr. Harold Stone. 17:53
The total number of media used was nine and will be retained by Veritext legal solutions. 17:53
STENOGRAPHIC REPORTER: You would like it in two days? 17:54
MR. TEZYAN: Yes, please. 17:54
STENOGRAPHIC REPORTER: Mr. Rueckheim, did you need it in two days? 17:54
MR. RUECKHEIM: We'll do the same. 17:54
(WHEREUPON, the deposition ended at 5:54 p.m.) 17:54
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CERTIFICATE OF STENOGRAPHIC REPORTER

I, ANDREA M. IGNACIO, hereby certify that the witness in the foregoing remote deposition was by me sworn to tell the truth, the whole truth, and nothing but the truth in the within-entitled cause;

That said remote deposition was taken in shorthand by me, a disinterested person, at the time and place therein stated, and that the testimony of the said witness was thereafter reduced to typewriting, by computer, under my direction and supervision;

That before completion of the deposition, review of the transcript [ ] was [x] was not requested. If requested, any changes made by the deponent (and provided to the reporter) during the period allowed are appended hereto.

I further certify that I am not of counsel or attorney for either or any of the parties to the said deposition, nor in any way interested in the event of this cause, and that I am not related to any of the parties thereto.

Dated: June 27, 2023

ANDREA M. IGNACIO, RPR, CRR, CCRR, CLR, CSR No. 9830

MICHAEL TEZYAN, Esq.
mtezyan@irell.com

June 27, 2023

RE: NETLIST, INC. vs. MICRON TECHNOLOGY, INC.
JUNE 26, 2023, HAROLD STONE, Ph.D., JOB NO. 5968770

The above-referenced transcript has been completed by Veritext Legal Solutions and review of the transcript is being handled as follows:

__ Per CA State Code (CCP 2025.520 (a)-(e)) – Contact Veritext to schedule a time to review the original transcript at a Veritext office.

__ Per CA State Code (CCP 2025.520 (a)-(e)) – Locked .PDF Transcript - The witness should review the transcript and make any necessary corrections on the errata pages included below, notating the page and line number of the corrections. The witness should then sign and date the errata and penalty of perjury pages and return the completed pages to all appearing counsel within the period of time determined at the deposition or provided by the Code of Civil Procedure.

__ Waiving the CA Code of Civil Procedure per Stipulation of Counsel - Original transcript to be released for signature as determined at the deposition.

__ Signature Waived – Reading & Signature was waived at the time of the deposition.

__ Federal R&S Requested (FRCP 30(e)(1)(B)) – Locked .PDF Transcript - The witness should review the transcript and make any necessary corrections on the errata pages included below, notating the page and line number of the corrections. The witness should then sign and date the errata and penalty of perjury pages and return the completed pages to all appearing counsel within the period of time determined at the deposition or provided by the Federal Rules.

xx Federal R&S Not Requested - Reading & Signature was not requested before the completion of the deposition.